Serial versus Parallel Data Transfers

OUTLINE:

- **Shift Registers**
- **Converting data from Serial $\longleftrightarrow$ Parallel**

Costas Foudas, Imperial College,
Rm: 508, x47590

Shift Registers

Shift Registers convert numbers expressed in terms of several bits (*many signal lines*) into a stream of 0, 1 and a Clock.

Advantage: A convenient way to reduce the number of Electrical signal lines by factors of 8, 16, 32, 64.

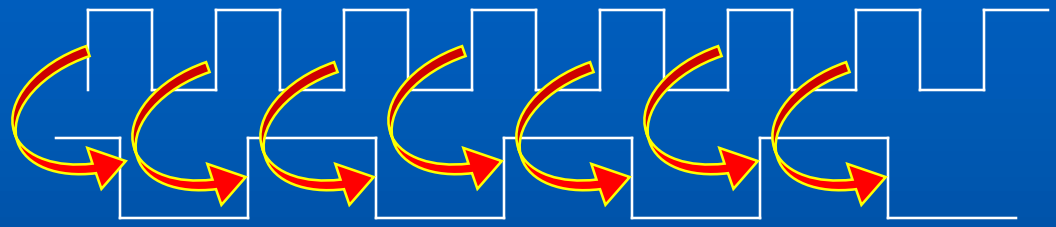
Disadvantage: For the same transfer rate the electronics must be faster by factors of 8, 16, 32, 64.

What do Shift Registers Do ?

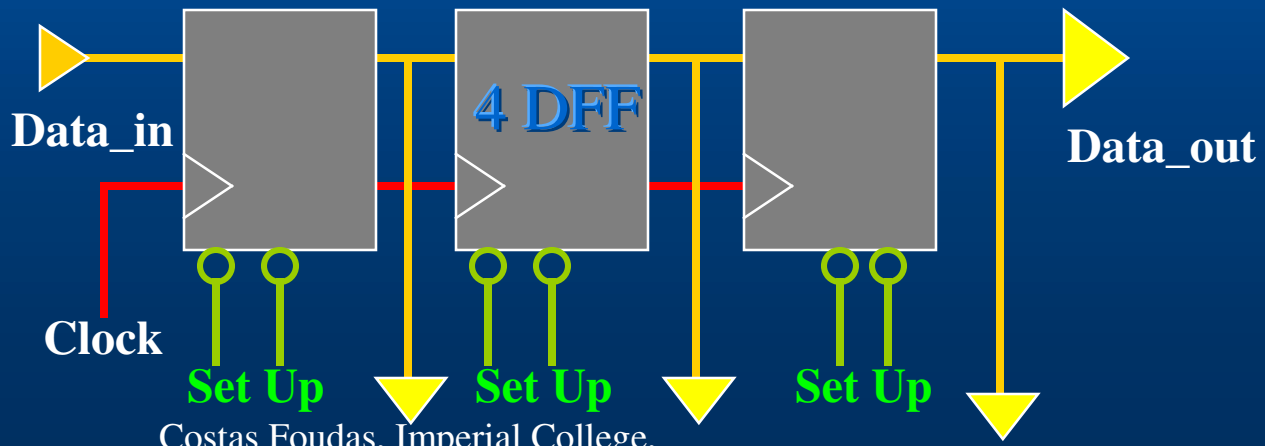
$AA

D7	H
D6	L
D5	H
D4	L
D3	H
D2	L
D1	H
D0	L

Set Up



D7	D6	D5	D4	D3	D2	D1	D0
H	L	H	L	H	L	H	L



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Suppose you feed an '1':

	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	0	0	0	0	0
T	1	0	0	0	0	0	0	0
2T	1	1	0	0	0	0	0	0
3T	1	1	1	0	0	0	0	0
4T	1	1	1	1	0	0	0	0
5T	1	1	1	1	1	0	0	0
6T	1	1	1	1	1	1	0	0
7T	1	1	1	1	1	1	1	0
8T	1	1	1	1	1	1	1	1

The 74HC165 Shift Register

Serial Data In

8-bit Word

Serial Data Out

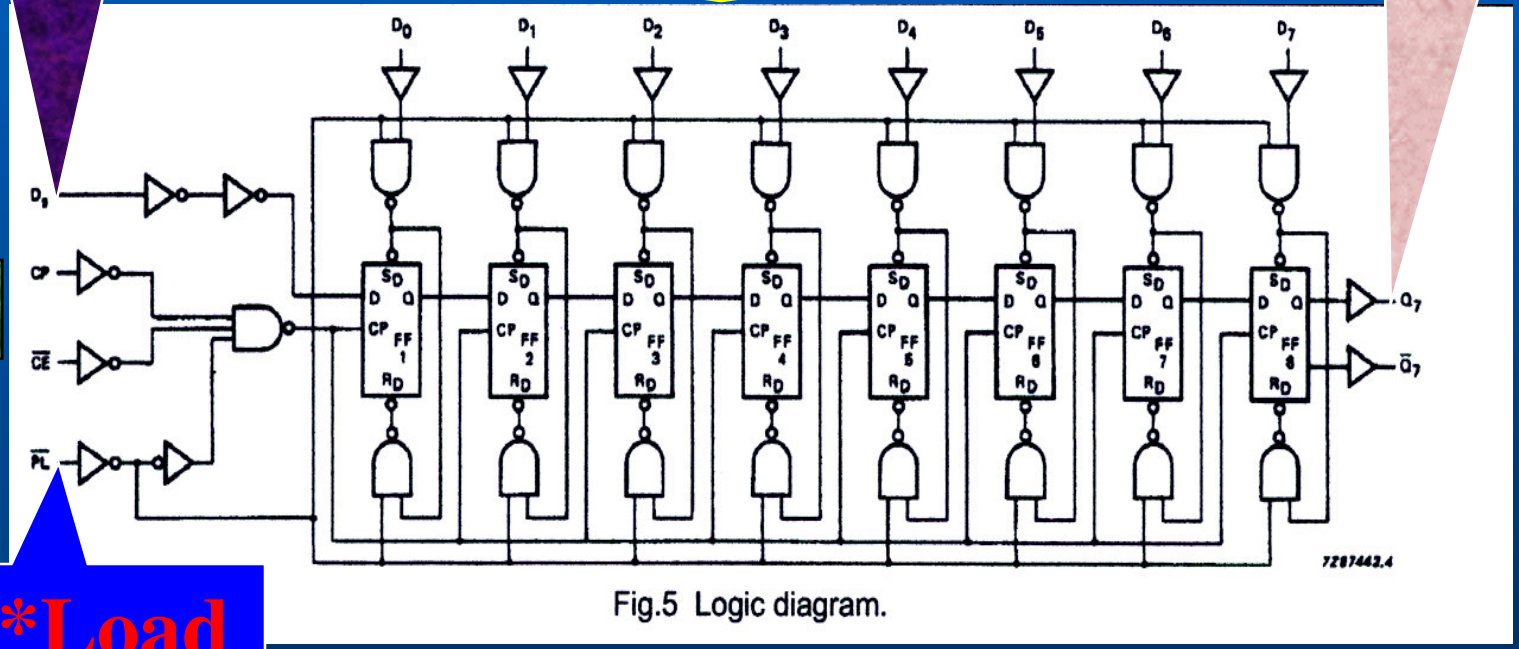

Fig.5 Logic diagram.

Clock

*Load

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The 74HC165 data

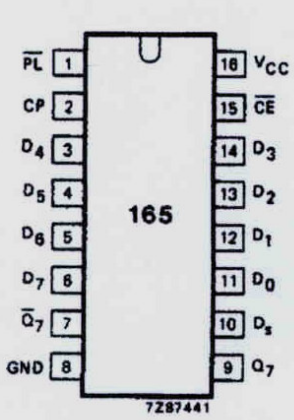


Fig.1 Pin configuration.

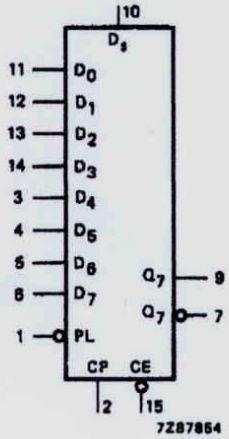


Fig.2 Logic symbol.

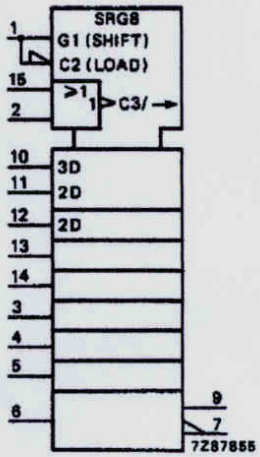


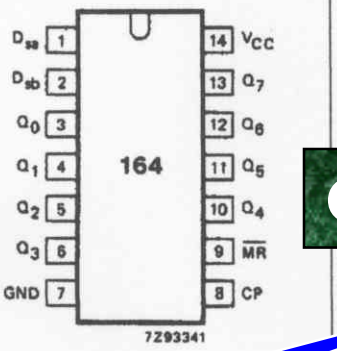
Fig.3 IEC logic symbol.

FUNCTION TABLE

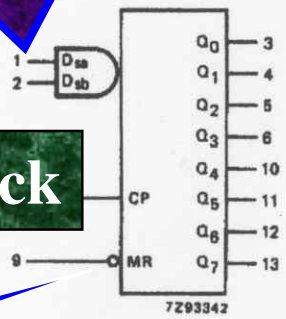
OPERATING MODES	INPUTS					Q_n REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q}_7$
parallel load	L L	X X	X X	X X	L H	L H	L - L H - H	L H	H L
serial shift	H H	L L	↑ ↑	l h	X X	L H	q_0-q_5 q_0-q_5	q_6 q_6	$\overline{q}_6$ q_6
hold "do nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	q_7

The 74HC164 Shift Register

Serial Data In

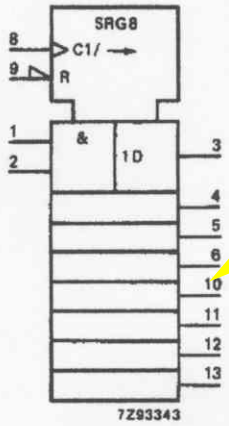


Clock



*Load

Fig.2 Logic symbol.



Parallel out

Fig.3 IEC logic symbol.

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
reset (clear)	L	X	X	X	L	L – L
shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

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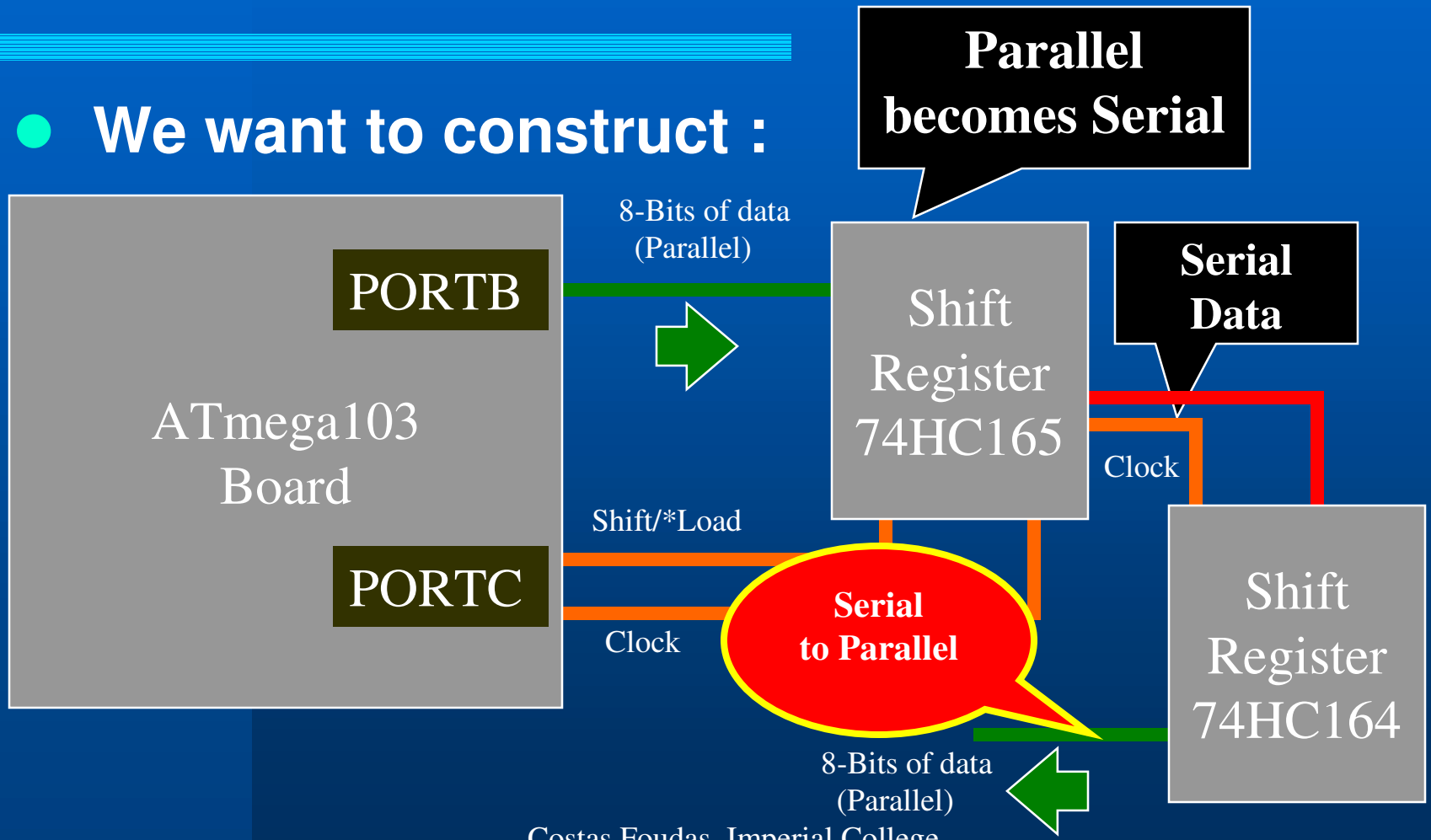
Rm: 508, x47590

High Level Design

- **We want to construct :**



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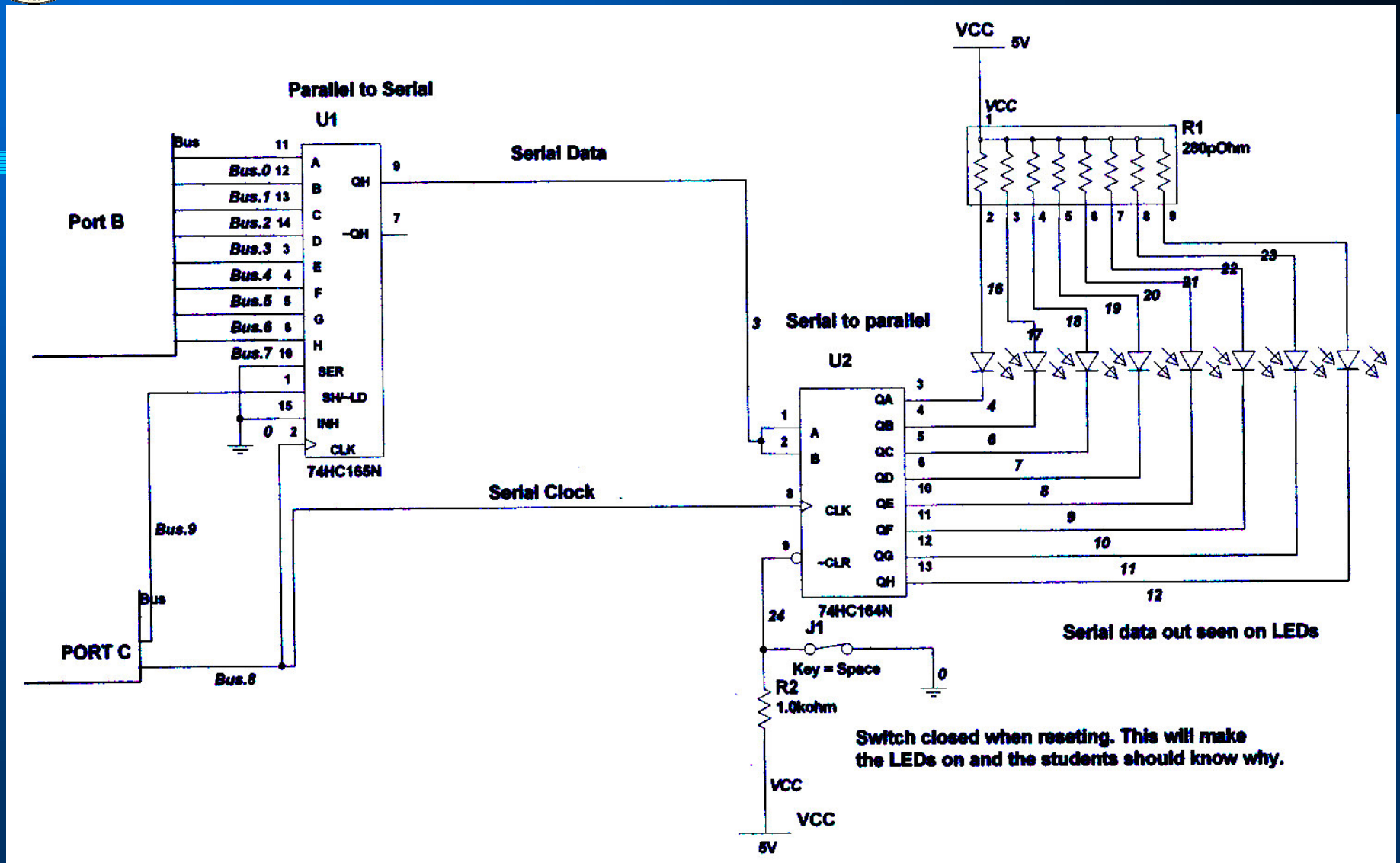
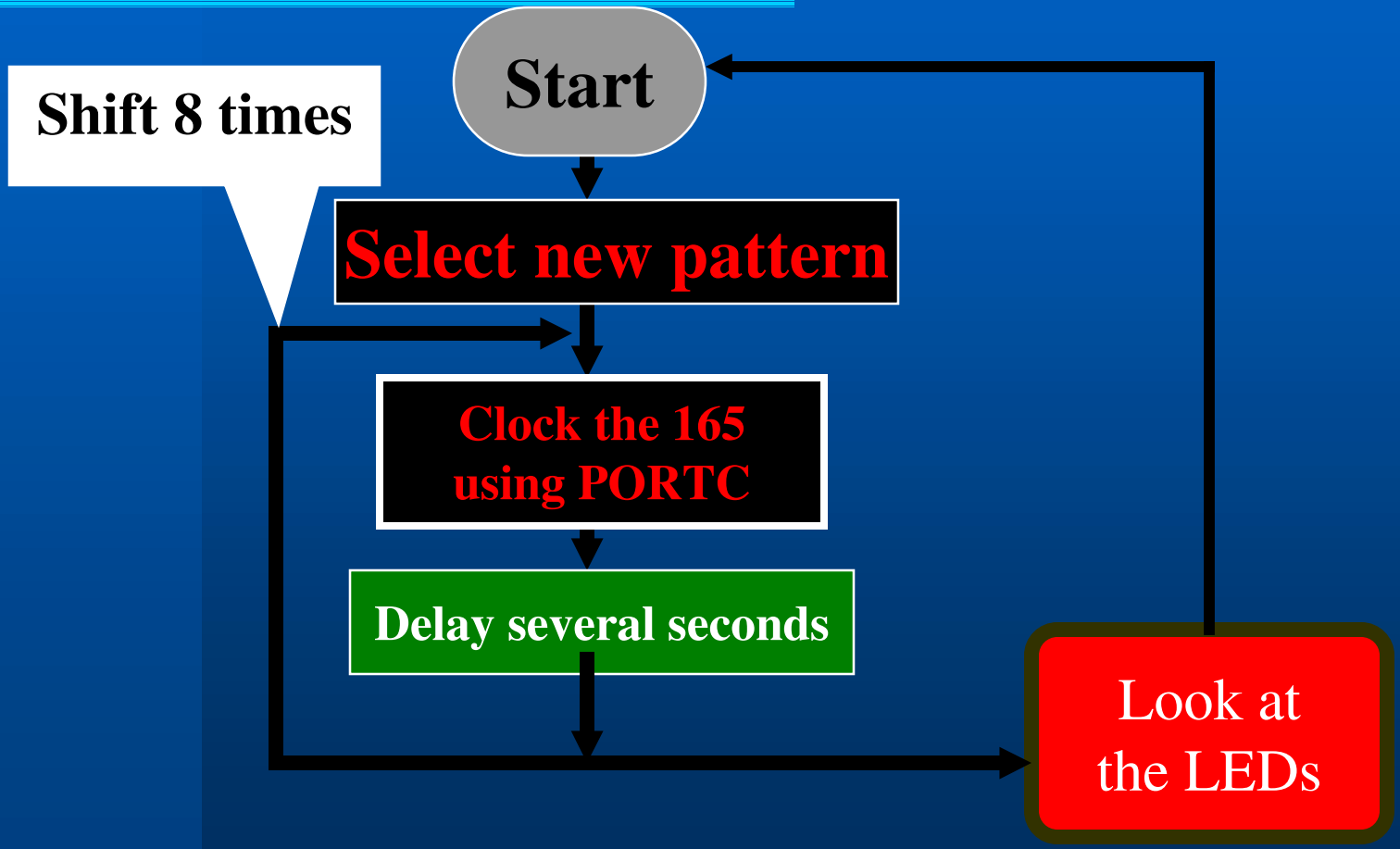
Low Level Design



The Memory Test Program



Task Plan:

(1) Construct a device that would turn the 8-bit parallel data from Port-B to serial data + clock .

(2) Construct a device that would receive the serial data, convert them to parallel data and display them using LEDs.

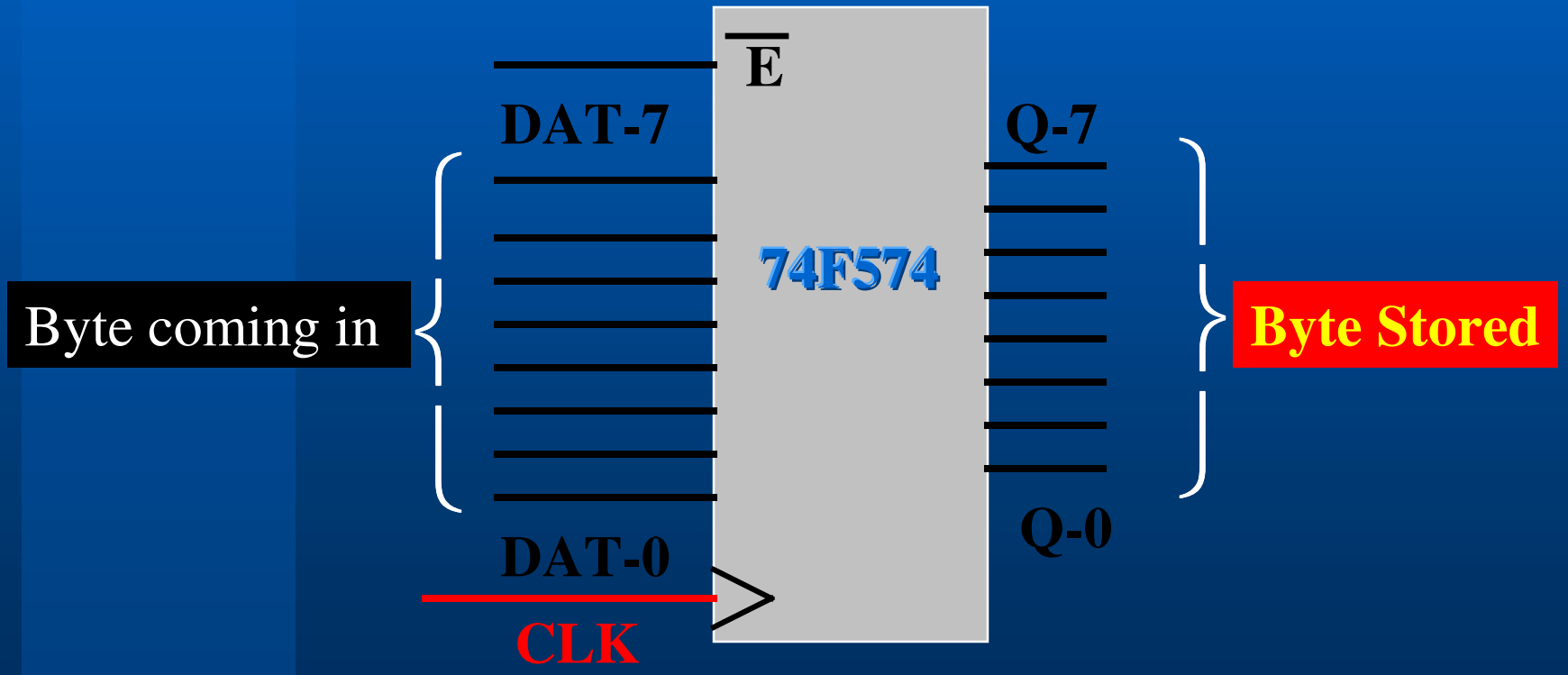
(3) Write a program that would send several patterns down your ‘serial link’ and demonstrate that it works.

For more motivated students:

I. You can attempt storing your data to a register at the end before sending them to the LEDs.
II. This will require knowledge on how a register really works
III. Next few slides describe the 75HC574 register with 3-state outputs.

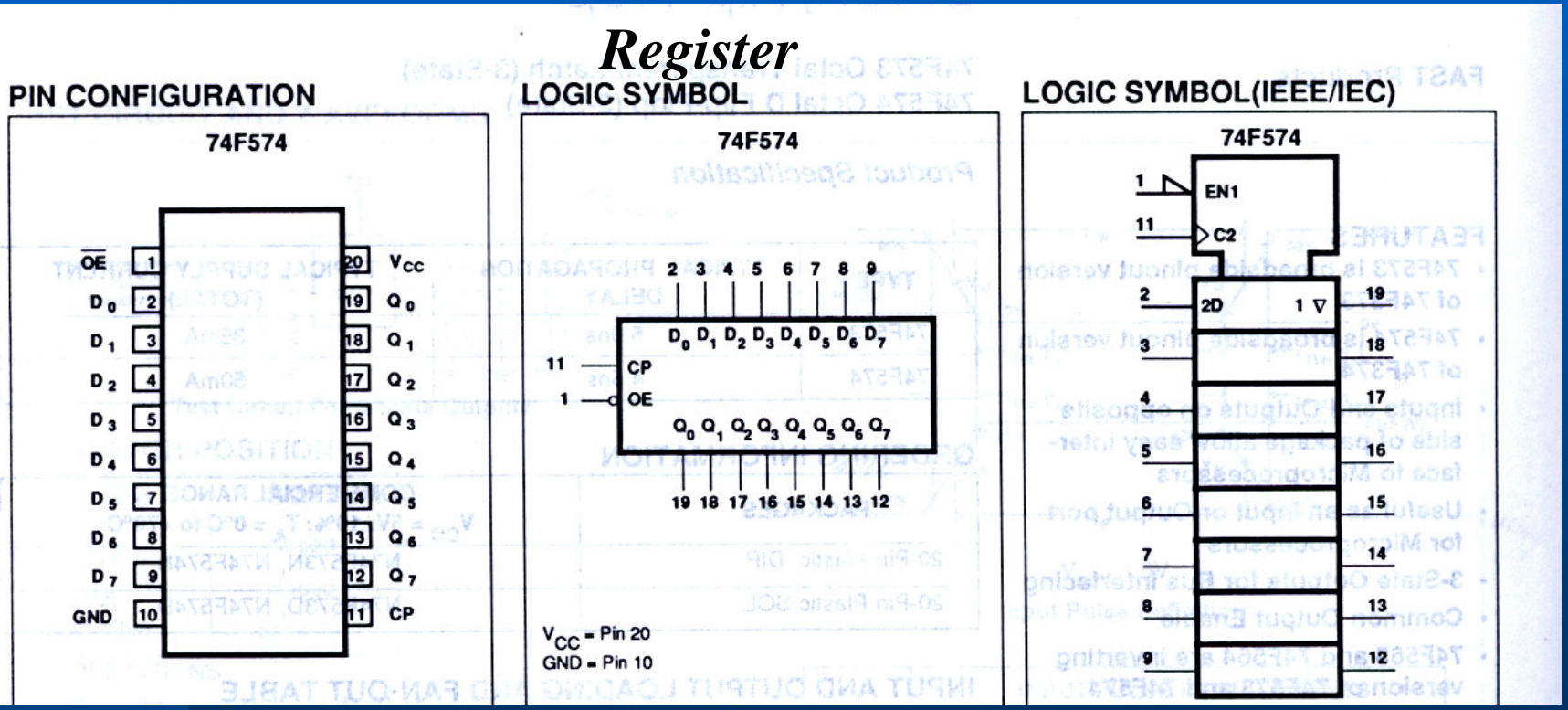
Guess what is the 1 Byte memory ?

- **It exists in one package :**

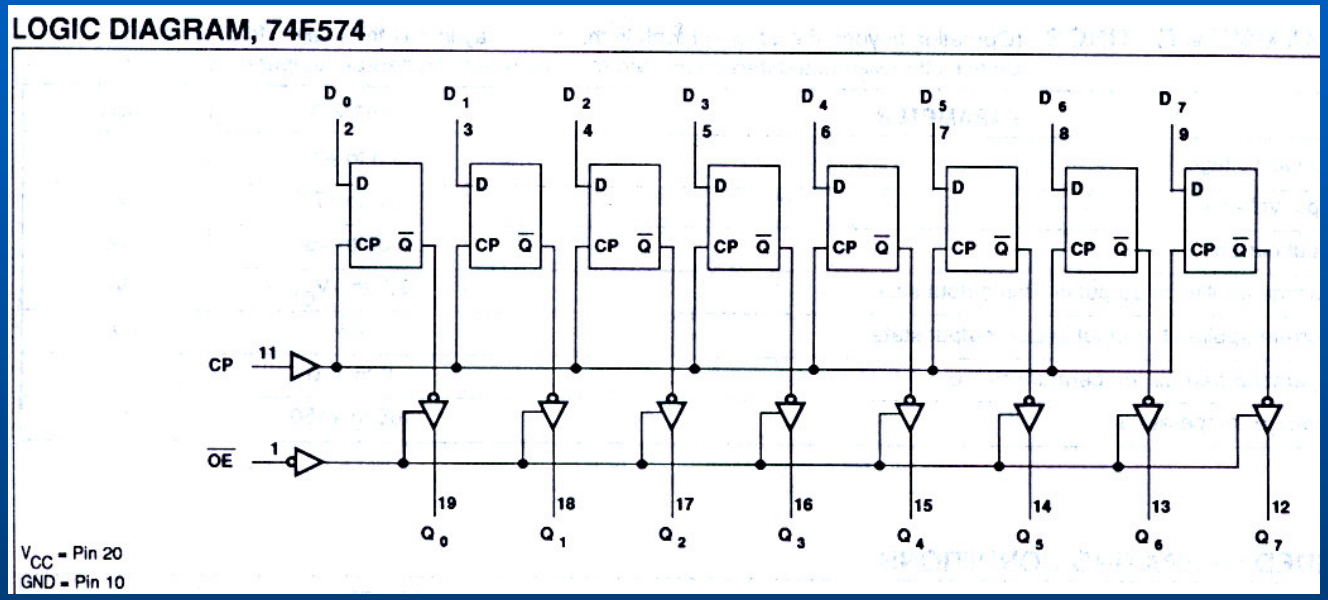


The data sheets of the 74F574

Register



What does the 74F574 do ?



The outputs of the 574 are tri-state : They Can be high ‘1’, low ‘0’, and DISCONNECTED (HIGH IMPEDANCE STATE).

The 74F574 Truth Table

FUNCTION TABLE, 74F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↑	D_n	D_n	Z	Disable outputs
H	X	X	X	Z	

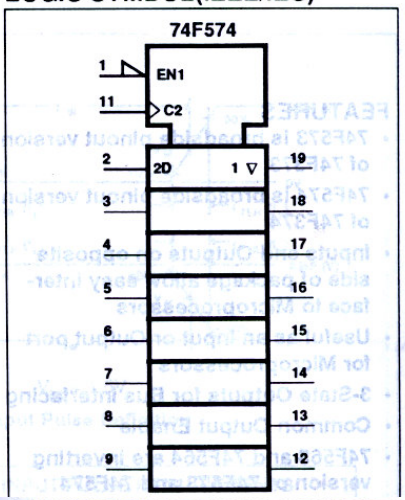
H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

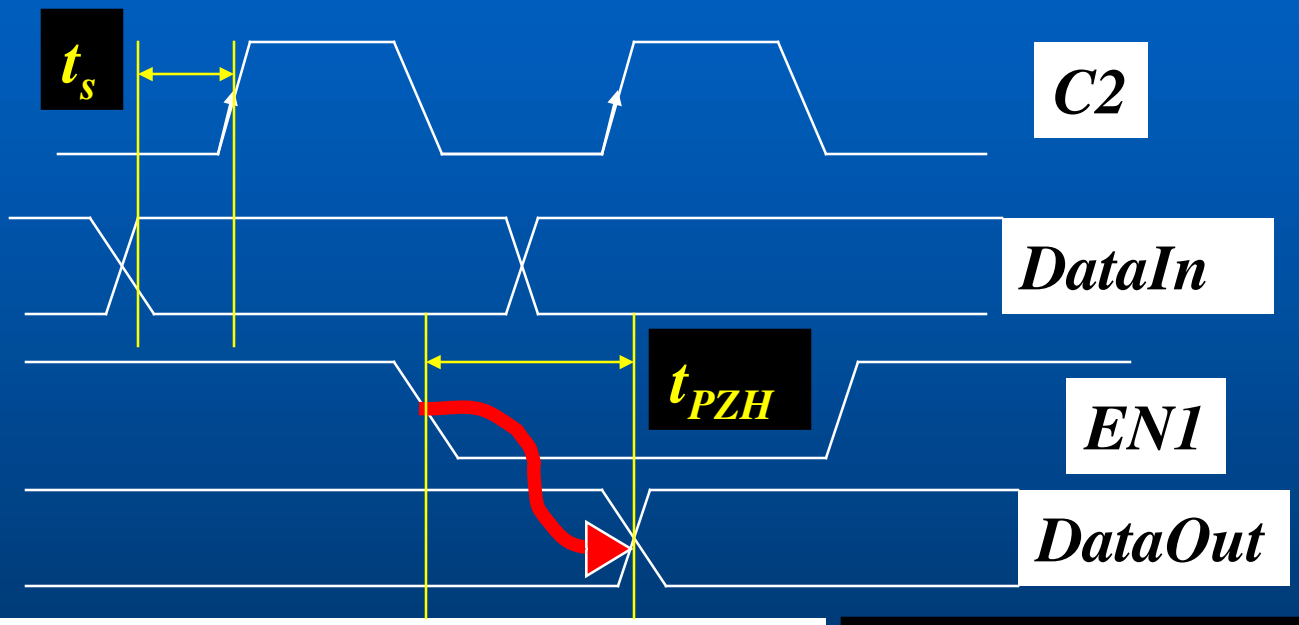
Costas Foudas, Imperial College,
Rm: 508, x47590

The Data Sheets of the 74F574 I

Register

LOGIC SYMBOL(IEEE/IEC)





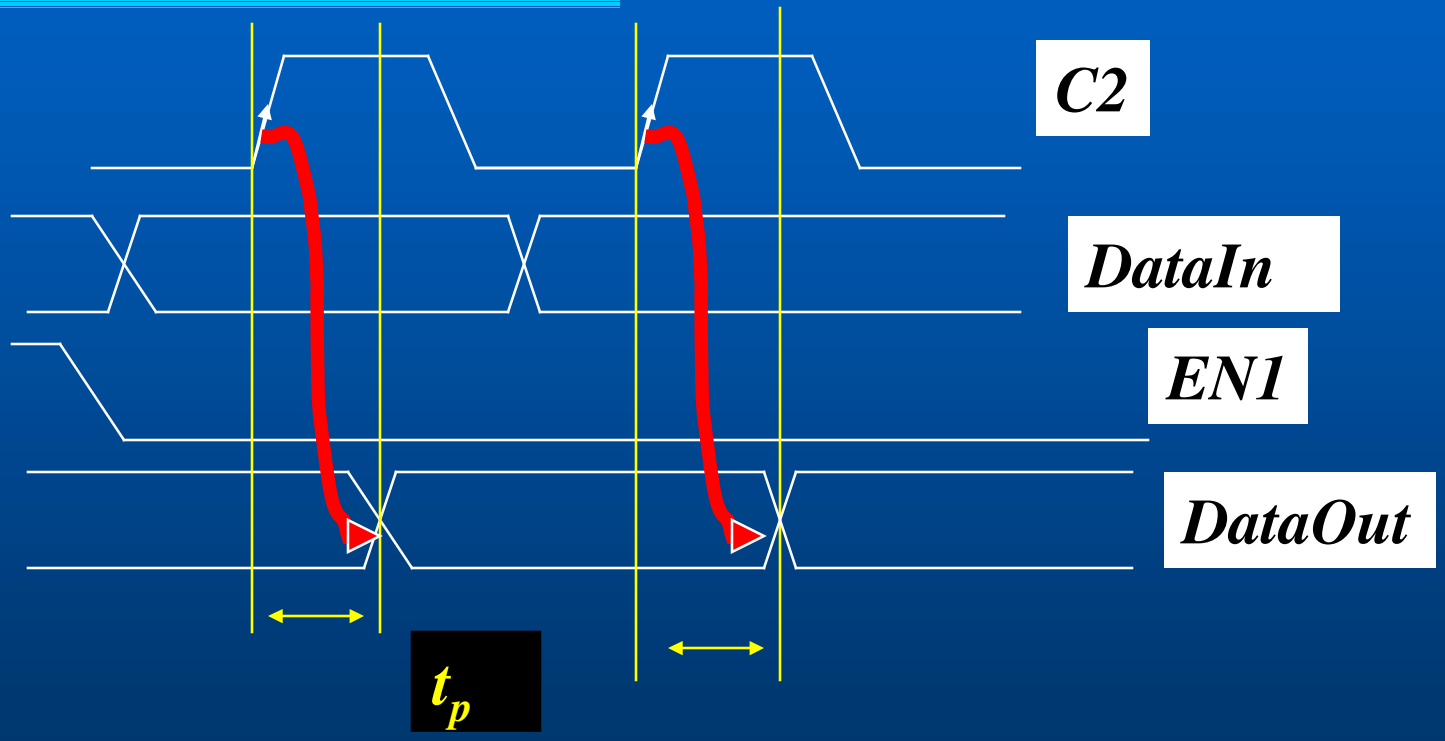
FUNCTION TABLE, 74F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	↑ X	D_n X	D_n X	Z Z	Disable outputs

T_s = setup time

t_{PZH} = Output Enable time

The Data Sheets of the 74F574 II



T_p = propagation delay

Task II:

(1) Construct the following circuit:

(2) Make sure that after clocking the serial data eight times you also clock the data in to the register.