Xilinx Power Estimator User Guide

UG440 (v2013.3/14.7) October 2, 2013

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/20/2013	2013.1/14.5	Revisions to manual for 2013.1/14.5 release: In Opening XPE, added information indicating that Microsoft Excel 2010 is supported in this release of XPE. In Settings Panel section, added information about the Default setting for **Optimization** in the **Settings** panel. In PS Sheet (Zynq-7000 Only), added a description of the new AXI Interfaces section on the PS sheet.
06/19/2013	2013.2/14.6	Revisions to manual for 2013.2/14.6 release: Updated screen display in Figure 21 to match 2013.2/14.6 version of the Summary sheet. In PS Sheet (Zynq-7000 Only), added that the DDR3L memory interface is now supported as a **Memory Type** on the PS sheet.
10/02/2013	2013.3/14.7	Revisions to manual for 2013.3/14.7 release: In Importing Data into XPE, added that you can now choose to include activity rates or not when you import an .xpe file from the Vivado Design Suite. In Importing Data into XPE, added that imported information will be displayed hierarchically in the Logic, BRAM, and DSP sheets. Updated screen display in Figure 21 to match 2013.3/14.7 version of the Summary sheet. In Setting BRAM Mode for Improved Accuracy, detailed the different BRAM write mode options in True dual-port mode and Simple dual-port mode.

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XILINX

Using Xilinx Power Estimator

Introduction

The Xilinx Power Estimator (XPE) spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project. XPE assists with architecture evaluation, device selection, appropriate power supply components, and thermal management components specific for your application.

XPE considers your design's resource usage, toggle rates, I/O loading, and many other factors which it combines with the device models to calculate the estimated power distribution. The device models are extracted from measurements, simulation, and/or extrapolation.

The accuracy of XPE is dependent on two primary sets of inputs:

- Device utilization, component configuration, clock, enable, and toggle rates, and other information you enter into the tool
- Device data models integrated into the tool

For accurate estimates of your application, enter realistic information which is as complete as possible. Modeling a certain aspect of the design over conservatively or without sufficient knowledge of the design can result in unrealistic estimates. Some techniques to drive the XPE to provide worst-case estimates or typical estimates are discussed in this document.

XPE is a pre-implementation tool for use in the early stages of a design cycle or when the RTL description is incomplete. After implementation, the XPower Analyzer (XPA) tool (in the ISE® Design Suite) or the Vivado® power analysis feature (in the Vivado Design Suite) can be used for more accurate estimates and power analysis. For more information about XPA, see the *XPower Analyzer Help* [Ref 1]. For more information about the Vivado power analysis feature, see the *Vivado User Guide: Power Analysis and Optimization (UG907)* [Ref 2].

XPE is a spreadsheet, so all Microsoft Excel functionality is fully retained in the writable or unprotected sections of the spreadsheet. XPE has additional functionality oriented towards ease of use. The drop-down menus and the comment-enabled cells are helpful features guide you.

The XPE spreadsheet also includes the Quick Estimate Wizard, the Memory Interface Configuration Wizard, the Memory Generator Wizard (for block memory and distributed memory), and the Transceiver Configuration Wizard. These wizards help novice and expert users to quickly enter the important configuration parameters, which will then generate relevant lines in the I/O, Logic, Block RAM (BRAM), Transceiver, and Other sheets, helping with accurate power analysis.

Getting Started with XPE

Opening XPE

1. XPE requires a licensed version of Microsoft Excel 2003, Microsoft Excel 2007, or Microsoft Excel 2010 to be installed.

   Microsoft Excel 2010 is officially supported in this release of XPE.

   OpenOffice and Google Docs spreadsheet editors are not supported in this release of XPE.

2. Download the latest available spreadsheet for your targeted device. The XPE spreadsheets are available at the Power Advantage webpage here:

   http://www.xilinx.com/power

   Note: The 7 series/Zynq®-7000 XPE spreadsheet is available in either .xlsm (Excel Macro-Enabled Workbook) or .xls (Excel 97-2003 Workbook) format.

TIP: *If you want to open a 7 series/Zynq®-7000 XPE spreadsheet in Microsoft Excel 2010, download the ..xlsm (Excel Macro-Enabled Workbook) format 7 series/Zynq®-7000 XPE spreadsheet.*

3. Make sure your Microsoft Excel settings allow macro executions. XPE uses several macros built into the XPE spreadsheet.
   - **Microsoft Excel 2010** - The following steps are required:
     a. From the XPE spreadsheet select **File > Options**.
     b. In the Excel Options dialog box, click on **Trust Center**.
     c. In the Trust Center dialog box, click on **Trust Center Settings** and select the **Macro Settings** tab.
     d. Select **Enable all macros**, then click **OK**.
     e. Reopen the XPE spreadsheet.
   - **Microsoft Excel 2007** - The following steps are required:
     a. From the Microsoft Office button select **Excel Options**.

b. In the Options dialog box, click on **Trust Center**.

c. In the Trust Center dialog box, click on **Trust Center Settings** and select the **Macro Security** tab.

d. Select **Enable all macros**, then click **OK**.

e. Open or, if already open, reopen the XPE spreadsheet.

Note: The 7 series/Zynq®-7000 XPE spreadsheet is available in either .xlsm (Excel Macro-Enabled Workbook) or .xls (Excel 97-2003 Workbook) format.

TIP: *You can save an Excel 2007 or later spreadsheet as an .xlsm file (Macro Enabled Workbook), and this will enable macro content. Calculations in XPE will not be affected if you decide to change to this extension. You can also enable the macro content each time you open the workbook. Enabling macro content by changing the Trust Center settings is a potentially dangerous way of enabling macro content.*

IMPORTANT: *If you save an Excel 2007 or later spreadsheet as an .xlsx file (Excel Workbook) you will lose the macro capability and render XPE nonfunctional. You will be warned of this if you try to save as an .xlsx file.*

- **Microsoft Excel 2003** - By default, the macro security level is set to High, which disables macros. To change the macro security level, follow these steps (actual menu names will vary with language of Microsoft Excel):

  a. On the Tools menu, point to **Macro** and click **Security**.

  b. In the Security dialog box, click the **Security Level** tab.

  c. Select **Medium**, then click **OK**.

  d. Open or, if already open, reopen the XPE spreadsheet.

  e. When prompted whether to enable or disable macros, click **Enable Macros**.

Minimum User Input Required

Power estimation for programmable devices like FPGAs is a complex process, since it is highly dependent on the amount of logic in the design and the configuration of that logic. To produce accurate estimates, the power estimation process requires accurate input values, such as resource utilization, clock rates, and toggle rates. To supply the minimum input that will allow XPE to estimate power with reasonable accuracy, you need the following:

- A target device-package-grade combination
- A good estimate of resources you expect to use in the design (for example, flip-flops, look-up tables, I/Os, block RAMS, DCMs, etc.)
- The clock frequency or frequencies for the design

- An estimate of the data toggle rates for the design
- The external memory and transceiver based interfaces with their data rates for the design
- The thermal environment in which the design will be operating

As a general rule, input as much information about your design as available, then leave the remaining settings to default values. This strategy will allow you to determine the device power supply and heat dissipation requirements.

TIP: *Use Excel formulas to link different cells together. For instance type '=CLOCK!E9' in the Logic sheet lines which list the resources driven by this clock domain.*

XPE Calculations and Results

XPE uses your design and environmental input, then combines this information with the device data model to compute and present an estimated distribution of the power in the targeted device.

XPE presents multiple views of the power distribution.

- **Power by Voltage Supplies** - For each required voltage source, this information is useful to select and size power supply components such as regulators, etc. Supply power includes both off-chip and on-chip dissipated power.
- **Power by User Logic Resources** - For each type of user logic in the design, XPE reports the expected power. This allows you to experiment with architecture, resources, and implementation trade-off choices in order to remain within the allotted power budget.
- **Thermal Power** - XPE lets you enter device environment settings and reports thermal properties of the device for your application, such as the expected junction temperature. With this information you can evaluate the need for passive or active cooling for your design.

The Summary sheet in XPE shows the total power for the device. Other sheets show usage-based power. Leakage within the unused portion of the considered resource (if any) is not shown.

The following sections provide more details on how to enter settings and review results.

Definitions/Terminology

Supported Device Families

Separate spreadsheets are available depending on the targeted architecture. These spreadsheets are updated when new device data become available or when new features are added to XPE.

- 7 Series FPGAs and Zynq-7000 AP SoCs
  - Artix™-7, Artix-7 Automotive grade, and Artix-7 Defense grade
  - Kintex™-7 and Kintex-7 Defense grade
  - Virtex®-7 and Virtex-7 Defense grade
  - Zynq®-7000, Zynq-7000 Automotive grade, and Zynq-7000 Defense grade
- Virtex-6 and Virtex-5 FPGAs
  - Virtex-6, Virtex-6 Low Power, and Virtex-6Q Defense grade
  - Virtex-5, Virtex-5Q Defense grade, and Virtex-5QV Space grade
- Virtex-4
- Spartan®-6 and Spartan-3A – This spreadsheet includes all sub-families, including Spartan-6 Lower Power, Spartan-6 Automotive, Spartan-6Q Defense-grade, Spartan-3AN, and Spartan-3A DSP
- Spartan-3E
- Spartan-3

IMPORTANT: *Download the latest available spreadsheet from the Power Efficiency webpage on the Xilinx website at this location:* http://www.xilinx.com/products/technology/power.

Device Model Accuracy

The accuracy of the characterization data existing in the tool is reflected by accuracy designations in the **Characterization** field on the Summary sheet of XPE. For most FPGAs, the history of the accuracy designation is also displayed in the **Release** sheet. The accuracy designations are Advance, Preliminary, and Production.

Advance

The data integrated into XPE with this designation is based primarily on measurements and characterization data made on early production devices. A set of widely used device resources are included in the characterization. Characterization data is limited to these few

blocks. This data is typically available within a year of product launch. Although the data with this designation is considered relatively stable and conservative, some under-reporting or over-reporting may occur. Advance data accuracy is considered lower than the Preliminary and Production data.

Preliminary

The data integrated into XPE with this designation is based on complete early production silicon. Almost all the blocks in the device fabric are characterized. Data for most of the dedicated blocks like TEMAC and PCIe block are also characterized and integrated into XPE. The accuracy of power reporting is improved compared to Advance data.

Production

The data integrated into XPE with this designation is released after enough production silicon of a particular device family member has been characterized to provide full power correlation over numerous production lots. Characterization data for all blocks in the device fabric is included.

Total Power

The total FPGA power is calculated as follows:

Total FPGA power = Device Static + Design Static + Design Dynamic

The power estimates are modeled to account for temperature and voltage sensitivity. Ambient temperature and regulated voltage on the system can be keyed into the appropriate cells provided for that purpose.

Device Static Power

Also referred to as Leakage. Device static represents the transistor leakage power when the device is powered and not configured.

Design Static Power

Design static represents the additional power consumption when the device is configured but there is no switching activity. It includes static power in I/O DCI terminations, clock managers, etc.

For design static power calculations, XPE starts by assuming a blank bitstream. To "instantiate" design elements for the design static power calculations, you must enter the appropriate resource counts on the sheets with count fields and non-zero clock frequencies for the sheets without count fields. I/O termination must also be set to match the board and the design.

Design Dynamic Power

Design dynamic represents the additional power consumption from the user logic utilization and switching activity.

Activity Rates

XPE shows values for these types of activity rates:

- Toggle Rates
- Signal Rates

Toggle Rates

Providing accurate toggle rates in the various XPE sheets is essential to get quality power estimates. This information, however, may not be readily available at the stage in the design cycle where you enter data in XPE. Activity may be refined as the design gets more defined. Below are guidelines you can follow to help you enter design toggle activity.

- For synchronous paths, toggle rate reflects how often an output changes relative to a given clock input and can be modeled as a percentage between 0–100%. The max data toggle rate of 100% means that the output toggles every active clock edge. For instance, consider a free running binary counter with a 100MHz clock. For the Least Significant Bit you would enter 100% in the **Toggle Rate** column since this bit toggles every rising edge of the clock. For the second bit you would enter 50% since this bit toggles every other rising edge of the clock.
- For non-periodic or event-driven portions of designs, toggle rates cannot be easily predicted. An effective method of estimating average toggle rates for a given design is to segregate the different sections of the design based on their functionality or hierarchy and estimate the toggle rates for each of the sub-blocks. An average toggle rate can then be arrived at by calculating the average for the entire design or hierarchy. Most logic-intensive designs work at around 12.5% average toggle rate, which is the default toggle rate setting in XPE.

  It has been observed that designs with random data patterns as input generally have toggle rates between 10%-30%. However, designs with a lot of glitch logic can have toggle rates as high as or even higher than 50%. Glitch logic is generally classified as combinatorial functions which have a high probability of the output changing when any one input changes, such as an XOR gates or unregistered arithmetic logic (i.e. adders). Functions that use large amounts of such logic, such as error detection/correction circuitry, may exhibit higher toggle rates due to this. Designs with large amounts of control path logic, such as embedded designs, on average have lower toggle rates due to large sections of logic being inactive at any given time during operation.

In summary, the primary factors that have an appreciable impact on the toggle rate of a design are:

- Input data pattern - Random data pattern versus known patterns have an impact on the toggle rate.
- Control signals - Use or lack of control signals such as reset and clock enables.
- Design logic - High glitch XOR/CARRY logic, a highly pipelined design, or an embedded design have an impact on the toggle rate.

IMPORTANT: *In all the sheets which do not have a dedicated **Clock Enable** column make sure you scale the toggle rate to account for any signal which gates this logic. For example, if the data toggle rate is modeled at 50% but the synchronizing clock is enabled 50 percent of the time, the resulting toggle rate should be 25% (50% x 50%).*

IMPORTANT: *To appreciate what 100% toggle rate means, think of a constantly enabled toggle flip-flop (TFF) whose data input is tied High. The T-output of this flip-flop toggles every clock edge. Very few designs could possibly have an average toggle rate that high (100%).*

Note: The IO sheet has a column to specify signal **Data Rate**. Make sure you adjust the **Toggle Rate** and **Data Rate** columns accurately. For example, on an input signal which toggles on both edges of the clock you would enter **Toggle Rate** = **100%** and **Data Rate** = **DDR** (Dual Data Rate).

Signal Rates

Signal rate defines the number of millions of transitions per second for the element considered. This is a read-only column that appears on some of the XPE sheets (for example, the Logic, I/O, DSP, and Block RAM sheets). The general equation to calculate signal rate is:

Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Effective Toggle Rate (%)

Fanout

Fanout defined in XPE is similar to the fanout reported by the synthesis tool and can differ from the fanout reported by the implementation tool. This difference is expected because fanout will vary with placement and packing of the logic.

- In XPE fanout represents the number of individual loads or logic elements the considered element is connected to (LUTs, flip-flops, block RAM, I/O flip-flops, distributed RAM, and shift registers).
- In the implementation tool (ISE PAR Report), fanout is the number of SLICEs the considered net is routed to. A SLICE typically contains multiple logic elements and users generally do not control packing of the different elements into SLICEs. XPE algorithms will estimate this packing before calculating the power.

Effective ΘJA (C/W)

This coefficient defines how power is dissipated from the FPGA to the environment (device junction to ambient air). Typically this option is calculated by XPE, taking into account, among other things, the different environment parameters in the **Settings** panel of the Summary sheet. Entering a value in this field will override XPE calculations. Use this option if you have calculated this parameter by simulations. You may also want to use this feature to factor out environmental parameters when analyzing power differences with another spreadsheet in which environment settings have been set differently.

ΘSA (C/W)

ΘSA represents the heatsink to ambient air thermal resistance. By default XPE obtains this value from a representative selection of heatsink data matched to the device package, combined with the **Heat Sink** value you set (**Low Profile**, **Medium Profile**, or **High Profile**) and the **Airflow** value you set. The value used by XPE is shown in the **ΘSA** field on the Summary sheet.

The heatsink values for **Low Profile**, **Medium Profile**, and **High Profile** for the different device packages are defined in Table 1.

Table 1: **Heat Sink Profile Definitions in Xilinx Power Estimator**

Device Package	Heat Sink Height (mm)
FF324 (19 mm)	◦ **Low Profile** - 6.3 mm ◦ **Medium Profile** - 9.5 mm ◦ **High Profile** - 12.7 mm
FF484 (23 mm)	◦ **Low Profile** - 6.3 mm ◦ **Medium Profile** - 9.5 mm ◦ **High Profile** - 12.7 mm
FF665-676 (27 mm)	◦ **Low Profile** - 6.3 mm ◦ **Medium Profile** - 9.5 mm ◦ **High Profile** - 12.7 mm
FF784 (29 mm)	◦ **Low Profile** - 6.3 mm ◦ **Medium Profile** - 9.5 mm ◦ **High Profile** - 12.7 mm
FF1136-1158 (35 mm)	◦ **Low Profile** - 6.3 mm ◦ **Medium Profile** - 9.5 mm ◦ **High Profile** - 12.7 mm
FF1738-1760 (42.5 mm)	◦ **Low Profile** - 12.7 mm ◦ **Medium Profile** - 14.6 mm ◦ **High Profile** - 17.6 mm
FF1923-1933 (45 mm)	◦ **Low Profile** - 14.6 mm ◦ **Medium Profile** - 20.6 mm ◦ **High Profile** - 27.6 mm

If you have the ΘSA information for your system you can enter your specific value. First set the **Heat Sink** drop-down menu on the Summary sheet to **Custom**, then enter your **ΘSA** value.

ΘJB (C/W)

ΘJB represents the device junction to board thermal resistance. By default XPE estimates the junction to board thermal resistance based on standard JEDEC four-layer measurements. If you have done thermal simulations of your system you can enter your own specific value. First set the **Board Selection** drop-down menu on the Summary sheet to **Custom**, then enter your **ΘJB** value.

Junction Temperature (°C)

This field forces the value of the device junction temperature. XPE then adjusts the ambient temperature to meet the specified junction temperature. This option could be used when you need to work backward from a known or assumed worst case junction temperature and define the environment that would ensure this temperature is not exceeded.

User Interface

XPE has these spreadsheet sheets:

- The Summary sheet lets you enter and edit all device and environment settings. This sheet also displays a summary of the power distribution and provides buttons to import data into XPE, export results, and globally adjust settings.
- Other sheets allow you to enter usage and activity details for the different resource types available in the targeted device (for example, IO, Block RAM (BRAM), and Multi-Gigabit Transceivers (MGTs)). These sheets report design power based on the resource usage. Resource leakage power is shown on the Summary sheet.

TIP: *XPE is intended to be intuitive to the novice spreadsheet-user. For information about a cell in the spreadsheet, move the mouse over the comment indicators (red triangle at the top right corner of the title cells) to read the relevant notes for the intended use (see Figure 1).*

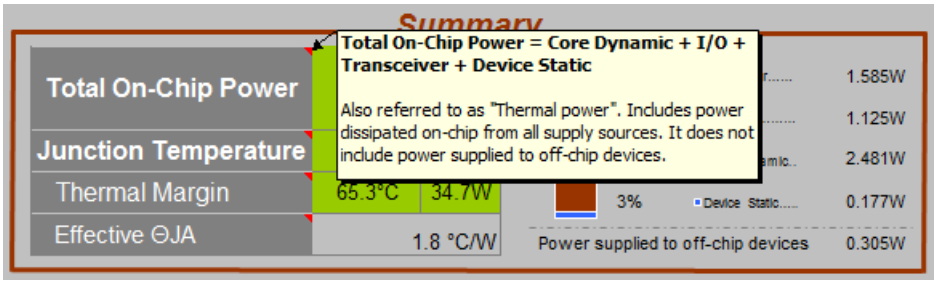


Figure 1: **Comment Indicators and Comment**

The XPE Toolbar

To make data entry into the tool easier, XPE supports importing data from different sources and allows settings to be changed globally. The toolbar is shown in Figure 2.

Note: The toolbar displayed below is the toolbar for the 7 series/Zynq-7000 XPE spreadsheet. Toolbar buttons for earlier architecture spreadsheets may have different names than the names displayed below.

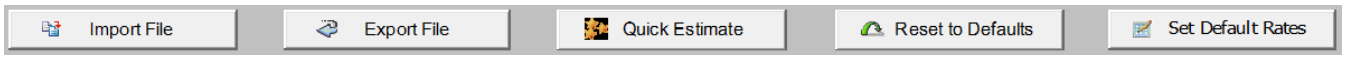


Figure 2: **XPE Toolbar (7 Series/Zynq-7000)**

Import File

Depending on what stage your design is in the FPGA development cycle, use this dialog box to import design information and activity into the spreadsheet. In the dialog box, select the **Files of type** field to determine whether you will import an .xls or .xlsm, .mrp, or .xpe file.

For a description of the import feature, see Importing Data into XPE, page 19.

Export File

The **Export File** button lets you export the following information from the current spreadsheet:

- The current settings for your design within XPE. These settings can be imported into an XPower Analyzer session within the ISE Design Suite.
- A text power report, which allows you to analyze the power information in the XPE spreadsheet in a textual format.

For a description of the export feature, see Exporting XPE Results, page 22.

Quick Estimate

The **Quick Estimate** button opens the Quick Estimate wizard. This wizard is a simple interface to allow novice and expert users to quickly enter the important parameters required for an accurate power analysis of a design implemented in a Xilinx device.

For a description of the Quick Estimate wizard, see Quick Estimate Wizard, page 24.

Reset to Defaults

The **Reset to Defaults** button resets all user settings to their default values, except for values in the **Device** selection table on the Summary sheet, and deletes all user entered values on the block details sheets (Clock, Logic, etc.).

Set Default Rates

This button opens up a dialog box which lets you change the default frequency, toggle rates or enable rates for the entire design or for specific sheets (see Figure 3).

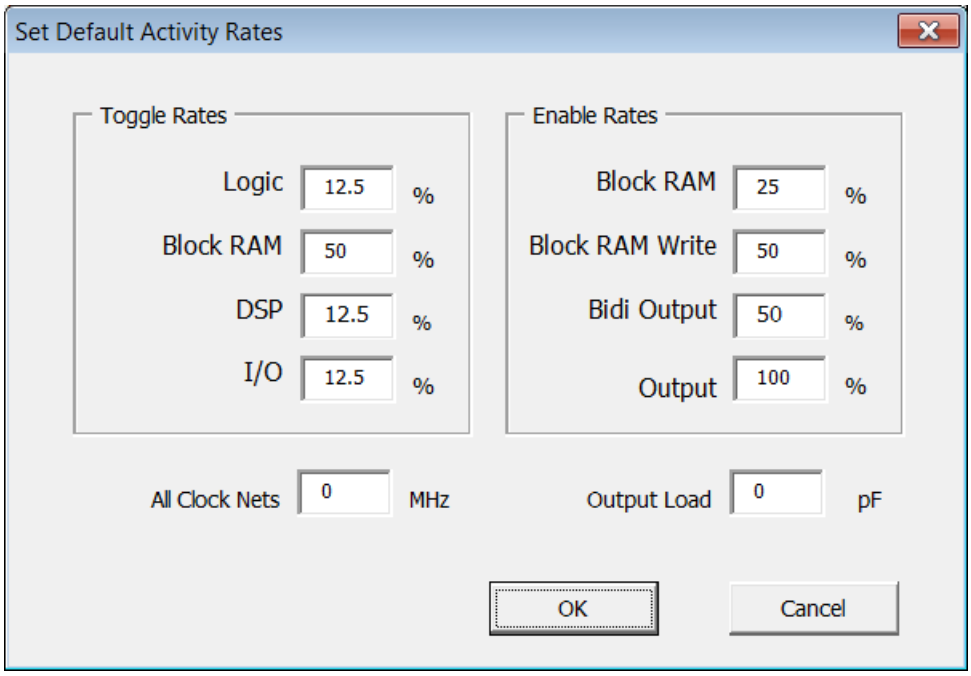


Figure 3: **Set Default Activity Rates Dialog Box**

The fields in the dialog box are:

- **Toggle Rates**

  Each field changes activity of the related sheet only. Acceptable range: 0 to 100%.

  To learn more about toggle rates, refer to Toggle Rates, page 10.

- **Enable Rates**

  Each field changes activity of the related sheet only. Acceptable range: 0 to 100%.

- **All Clock Nets**

  The clock frequency entered here applies to CLOCK, LOGIC, IO, BRAM and DSP sheets.

- **Output Load**

  The equivalent capacitance seen by the output driver for the routing and components connected to this board trace. This setting does not affect power calculations for inputs.

XPE Cell Color-Coding Scheme

To simplify data entry and review, the XPE cells are color coded. A color **Legend** appears at the bottom of the Summary sheet (see Figure 4).

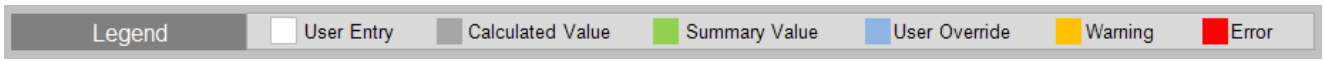


Figure 4: **Color Legend (Summary Sheet)**

A description of the spreadsheet's color-coding scheme is provided in Table 2.

Table 2: **XPE Cell Color-Coding Scheme**

Cell Color	Cell Use	Available User Action
White	Allows user to enter data	Editable
Grey	Displays a calculated value	Read-only
Green	Displays a summary value	Read-only
Blue	User override of cells normally calculated by XPE	Editable
Orange	Flags a warning. Indicates that a resource is not available.	Editable
Red	Flags an error. Examples of errors are: • A resource limit in the device has been exceeded. • The limits of a device specification (for example, junction temperature) have been exceeded.	Read-only. Edit other cells to correct the error.

Exchanging Power Information with XPower Analyzer

To determine device power supply requirements and estimate thermal dissipation throughout the design process, data exchange mechanisms are available between the different power estimation tools, Xilinx Power Estimator (XPE) and XPower Analyzer (XPA), which is in the ISE Design Suite (IDS). Details on the methodology and user flow are presented in the *Power Methodology Guide (UG786)* [Ref 2]. This data exchange mechanism is available for the Spartan-6, Virtex-6, Artix-7, Kintex-7, and Virtex-7 families.

- Export settings to XPower Analyzer

  In a typical development process you will first perform power estimation in XPE to size the voltage supply sources, evaluate thermal power dissipation paths, and allocate the total power budget to the different blocks in the FPGA system. Later in the development cycle you will want to perform post implementation power analysis in XPower Analyzer to validate against your power and thermal goals. Instead of manually re-entering this environmental data into XPA you can export to a file and have XPA read it for your next analysis. This process exports all environment, thermal, and voltage settings which in turn helps getting realistic power estimations in XPA that can easily be compared between the two tools.

  For step-by-step export instructions, see Exporting XPE Results, page 22.

- Import results from XPower Analyzer

  This flow is useful in the following cases:

  - The power reported in XPower Analyzer exceeds your requirements and you want to evaluate different scenarios, adjusting resources used, count, and configuration. You can also estimate power gains from techniques such as logic gating or resource time sharing, without modifying your code.
  - Your project uses (or reuses) IP blocks already implemented in a previous design or acquired. You can import these existing blocks into XPE to quickly get resource and power usage for these blocks. You can then focus your efforts in XPE to enter data for the new pieces of logic not yet defined.
  - Team-based design – A project manager can regularly monitor power for the entire design by integrating resource usage and power consumption for modules developed by the different teams.

  For step-by-step import instructions, see Importing Data into XPE, page 19.

Importing Results from Vivado Power Analysis

A data exchange mechanism is available to import data from the Vivado® power analysis feature into Xilinx Power Estimator (XPE). This data exchange mechanism is available for the Artix-7 (including Artix-7 Automotive), Kintex-7 Virtex-7, and Zynq-7000 families.

This flow is useful in the following cases:

- The power reported in the Vivado Design Suite exceeds your requirements and you want to evaluate different scenarios, adjusting resources used, count, and configuration. You can also estimate power gains from techniques such as logic gating or resource time sharing, without modifying your code.
- Your project uses (or reuses) IP blocks already implemented in a previous design or acquired. You can import these existing blocks into XPE to quickly get resource and power usage for these blocks. You can then focus your efforts in XPE to enter data for the new pieces of logic not yet defined.
- Team-based design - A project manager can regularly monitor power for the entire design by integrating resource usage and power consumption for modules developed by the different teams.

For step-by-step import instructions, see Importing Data into XPE, page 19.

Data Import and Export

Depending on the stage in the FPGA development cycle your design is in, XPE provides multiple mechanisms to simplify data entry and manage output data. These mechanisms use the data import and data export features of XPE.

The XPE import and export features are useful for exchanging power information with XPower Analyzer in the ISE® Design Suite (see Exchanging Power Information with XPower Analyzer) or importing results from the Vivado® power analysis feature in the Vivado Design Suite (see Importing Results from Vivado Power Analysis).

For step-by step instructions for importing or exporting XPE data, see the following:

- Importing Data into XPE, page 19.
- Exporting XPE Results, page 22.

Importing Data into XPE

In the Summary sheet, click the **Import...** button to open the dialog box shown in Figure 5. This dialog box varies slightly depending on device architecture, since newer family spreadsheets offer more import capabilities.

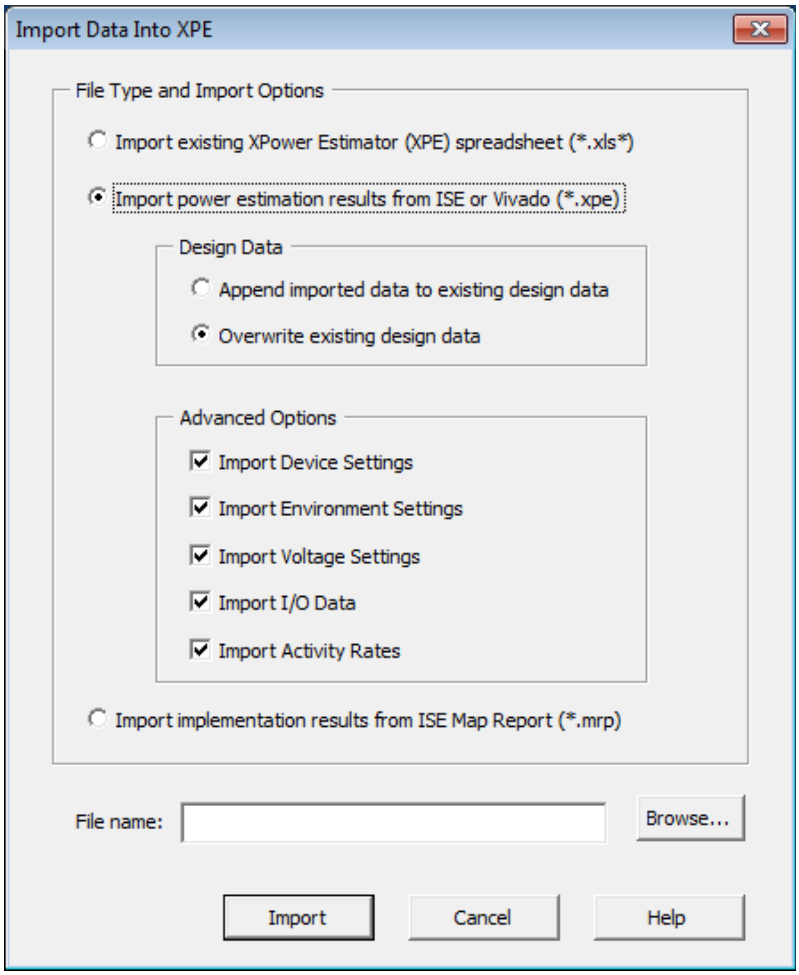


Figure 5: **Import Dialog Box (7 Series)**

This dialog box lets you select among the following import options:

- **Import existing Xilinx Power Estimator spreadsheet (*.xls*)**

  Use this option to import an existing XPE spreadsheet (.xls or .xlsm file). This option is useful when starting a new design which reuses previous IP blocks or when updating the design information into the latest spreadsheet version. This action deletes all data in the current spreadsheet, then imports all data from the selected spreadsheet.

IMPORTANT: *When the import is complete, make sure to verify and adjust the imported data where appropriate. For example, adjust utilization and resources count columns when porting a design to a new architecture.*

- **Import power estimation results From ISE or Vivado (*.xpe)**

  Use this option to further analyze your design by importing complete designs or IP blocks. The .xpe file you are importing can come from either the ISE Design Suite or the Vivado Design Suite.

  - ISE Design Suite - The .xpe file was produced by XPower Analyzer or by the **-xpe** option to the **xpwr** command. See the XPower Analyzer Help or the description of the **-xpe** option to the **xpwr** command line in the *Command Line Tools User Guide (UG628)* [Ref 4] for details on how to generate this interoperability file.
  - Vivado Design Suite - The .xpe file was produced by the report power tool or by the **-xpe** option to the **report_power** Tcl command. See the *Vivado User Guide: Power Analysis and Optimization (UG907)* [Ref 2] for details on how to generate this interoperability file.

  Benefits and use model for this flow are presented in Exchanging Power Information with XPower Analyzer, page 17 or Importing Results from Vivado Power Analysis, page 18.

  To import this data into the spreadsheet:

  a. In the Summary sheet of the XPE spreadsheet, click **Import File**.

  b. In the import dialog box, browse and select the `.xpe` file to import.

  c. (Optional. 7 series and Zynq-7000 devices only) In the **Design Data** section of the dialog box, select whether you want the imported data to override any previously entered data in the spreadsheet or rather append to the existing results.

  d. (Optional. 7 series and Zynq-7000 devices only) In the **Advanced Options** section of the dialog box, specify data to include during the import (**Device Settings**, **Environment Settings**, **Voltage Settings**, **I/O Data**, and **Activity Rates**).

TIP: *When you import an .xpe file from the Vivado Design Suite, the imported data will be displayed hierarchically in the Logic sheet, BRAM sheet, and DSP sheet. In Figure 6, the **Name** column in the Logic sheet contains a row for a parent module followed by rows with names indented, representing modules within the parent.*

Name	Clock (MHz)	LUTs as			Registers
		Logic	Shift Registers	Distributed RAMs	
top/cpuEngine					
Combinatorial	2.8	6595	0	0	0
clkgen/cpuClk	50.0	0	0	0	3333
clkgen/wbClk	50.0	0	0	0	506
top/fftEngine					
Combinatorial	24.2	1797	0	0	0
clkgen/fftClk	100.0	0	1	0	1339
clkgen/wbClk	50.0	0	0	0	116
top/mgtEngine					
Combinatorial	13.2	403	0	0	0
clkgen/wbClk	50.0	0	0	0	66
mgtEngine/gt_usrclk_source/GT0_TXUSR	78.1	0	0	0	144
mgtEngine/gt_usrclk_source/GT2_TXUSR	78.1	0	0	0	144
mgtEngine/gt_usrclk_source/GT4_TXUSR	78.1	0	0	0	144
mgtEngine/gt_usrclk_source/GT6_TXUSR	78.1	0	0	0	144

Figure 6: **Hierarchical Display of Imported Data (7 Series)**

- **Import Implementation Results from ISE Map Report (*.mrp)**

  Select the import from Map Report (.mrp file) when portions of the design have been implemented in the ISE Design Suite. You can import the exact resource count from a Map Report to get a more accurate power estimation after the design is placed. This flow is also used when portions of the design are implemented while others are still being designed, so you can add details for the expected remaining logic and evaluate the total design power distribution.

  Note: This process overwrites any utilization data, but preserves environment settings.

TIP: *After import you will notice resources used are grouped into a minimum set of lines. The map report only contains the counts of the various blocks and you will need to set the bit width, data rate, clock, mode, enable, and other configurations on each XPE sheet to match your design.*

TIP: *The I/O and BRAM sheets are populated based on unique configuration. I/Os are grouped by bus and all BRAMs with the same configuration appear on a single line. You may therefore need to add additional rows and adjust the counts to group by clock domain, module, or functionality.*

Exporting XPE Results

In the Summary sheet click the **Export File** button to open the dialog box shown in Figure 7.

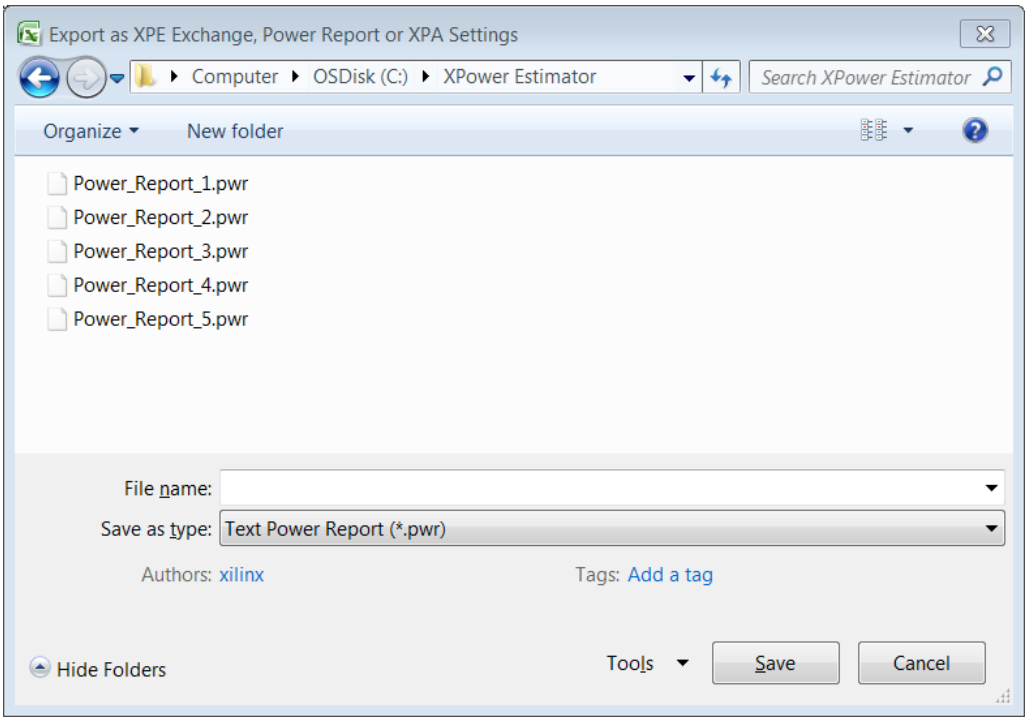


Figure 7: **Export Dialog Box**

In the dialog box the **Save as type** field lets you select among the following data formats:

- Export as **XPA Settings (*.xpa)** file

  Use this format to export XPE settings so they can then be applied to an XPower Analyzer session. This tool is typically used later in the design cycle when you are ready to perform a post place and route power analysis. The tool will create an .xpa file which contains all the environment settings, such as thermal, board and voltage properties. This simplifies the analysis setup in XPower Analyzer and ensures power data can be compared between the two tools.

  Note: To read the data exported from XPE into XPower Analyzer, enter the **Settings file** name (`*.xpa`) in the dialog box that appears when you open a design in XPower Analyzer (**File > Open Design**).

  Note: In the XPower (XPWR) command line tool, which performs a power analysis on your design within the ISE Design Suite, use the **`-x <file_name>`** switch to read in the XPE exported data.

- Export as **Text Power Report (*.pwr)**

Use this format to export XPE Summary sheet results in a text format. XPE will save all the information on the Summary sheet in a sequence of tables so the information is easy to read. This feature can be used to archive or compare multiple scenarios. It can also help if your design flow uses scripts to parse and use XPE results.

- Export as **XPE Exchange (*.xpe)** file (7 series and Zynq-7000 only)

  Use this format to export the contents of an XPE spreadsheet in a smaller file, and then restore it by importing it into another spreadsheet.

XPE Wizards (7 Series and Zynq-7000 Only)

The XPE wizards, available in the 7 series/Zynq-7000 Xilinx Power Estimator spreadsheet, are simple interfaces to allow novice and expert users to quickly enter the important parameters required for an accurate power analysis of a design implemented in a Xilinx device.

There are two types of XPE Wizards:

- Quick Estimate wizard - The Quick Estimate wizard populates the XPE sheets with information about your entire design, allowing XPE to perform a rough power estimate for the design. The Quick Estimate wizard is often used as the first step in specifying your design in XPE to determine its power requirements.
- IP Module wizards - The IP Module Wizards extend XPE to allow you to easily populate the XPE spreadsheet with information about:
  - Various types of external memory interfaces (for example, DDR3, DDR3L, LPDDR2, QDR+, and RLDRAM).
  - Transceiver based interfaces (for example, 10GBASE-R, Interlaken, PCIe, Aurora, and CPRI.
  - Block memory and distributed memory used in your design.

Quick Estimate Wizard

The Quick Estimate wizard populates the XPE sheets with information about your entire design, allowing XPE to perform a rough power estimate for the design. After you run this rough estimate using the Quick Estimate wizard, you can view the data the wizard entered, modify the spreadsheet entries the wizard created, and add entries of your own to describe your design more completely.

If you run the Quick Estimate wizard a second time, you will replace all the spreadsheet entries from the previous run with entries from the current run.

The following manuals will help you supply information to the Quick Estimate Wizard:

- *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5]
- *7 Series FPGAs Memory Resources User Guide (UG473)* [Ref 6]
- *7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7]
- *7 Series FPGAs GTP Transceivers User Guide (UG482)* [Ref 8]
- *7 Series FPGAs Memory Interface Solutions User Guide (UG586)* [Ref 9]

To populate the 7 Series XPE sheets using the Quick Estimate wizard:

1. In the Summary sheet **Settings Panel** specify the target part, including the **Speed Grade** and **Temp Grade**.
2. On the Summary sheet, click the Quick Estimate button.

3. In the XPE Quick Estimate dialog box, fill out the information in the dialog box for your design.

   The entries available in the dialog box depend on the Xilinx device in which you will implement your design.

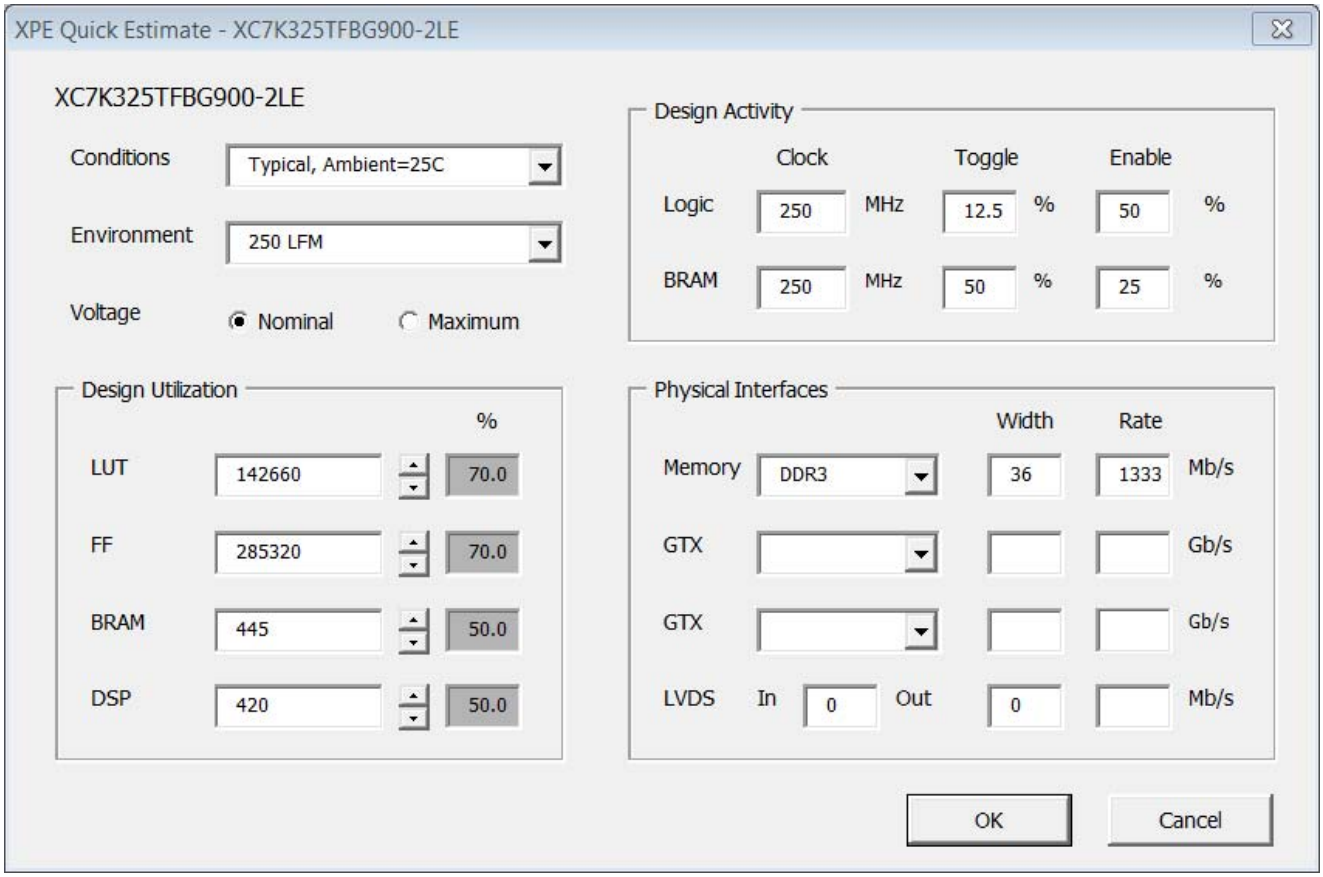


Figure 8: **XPE Quick Estimate Dialog Box (Virtex-7)**

The fields in the XPE Quick estimate dialog box are:

- **Conditions**

  This selection allows you to choose:

  - A **Typical** process and nominal voltages at the specified **Ambient** temperature.

    OR

  - A **Maximum** process and maximum voltages, with the **Junction** temperature set for a worst case power analysis at the specified temperature grade limit.

- **Environment**

  Allows you to select the airflow environment under which your device will operate (**Still Air**, **250 LFM**, or **250 LFM (w/Heatsink)**).

- **Voltage**

  Allows you to specify whether XPE will calculate power assuming the device is operating with all supplies at their **Nominal** or **Maximum** voltages.

- **Design Activity**

  For the **Logic** (configurable logic blocks (CLBs) and interconnect) and **BRAM** (block RAM), enter these values:

  - **Clock**

    Specify a single clock frequency, in MHz. The **Clock** frequency defaults to different values for the different device families (Artix-7 (including Artix-7 Automotive), Kintex-7, and Virtex-7), but you may set the **Clock** frequency to any value.

  - **Toggle**

    Enter a single **Toggle** rate (in %). This toggle rate will apply to all the resources in the **Logic** or to the **BRAM**.

  - **Enable**

    Enter a single **Enable** rate (in %). The **Enable** rate will apply to the slice clock enable in the **Logic** or to the **BRAM** enable.

- **Design Utilization**

  Enter the number of each resource (**LUT**, **FF**, **BRAM**, and **DSP**) you estimate your design will use.

  The **%** column shows the percentage of utilization for the resource in the specified device.

  You can enter a number in the box provided or use the spin buttons (the up and down arrowheads) to increase or decrease the utilization **%** by 5% each click.

  If you try to enter a value greater than the total number of the resource in the device (for example, you try to enter 10,000 LUTs for a device that only contains 9600 LUTs), the value displayed will change to the total number of the resource in the device (in this example, 9600 LUTs) and the utilization **%** will be 100%.

- **Physical Interfaces**

  For the memory interface (**Memory**) you specify, enter a bit width (**Width**) and a data rate (**Rate**) in Mb/s.

  For the transceiver interfaces (**GTP**, **GTX**, etc.) you specify, enter a bit width (**Width**) and a data rate (**Rate**) in Gb/s.

  For **LVDS**, specify the number of input pins (**In**), output pins (**Out**), and the data rate (**Rate**) in Mb/s.

4. When you have filled out the values for your design, click **OK**.

   After a DRC (Design Rules Check) runs, the sheets in Xilinx Power Estimator spreadsheet will be populated based on the values you entered, and XPE will estimate power for the design you specified.

IP Module Wizards

The IP Module wizards extend XPE to allow you to easily enter various types of external memory interfaces (e.g. DDR3, DDR3L, LPDDR2, QDR+, RLDRAM), transceiver based interfaces (e.g. 10GBASE-R, Interlaken, PCIe, Aurora, and CPRI) and block memory or distributed memory.

The IP Module wizards are:

- Memory Generator Wizard (for Distributed Memory)
- Memory Generator Wizard (for Block Memory)
- Memory Interface Configuration Wizard
- Transceiver Configuration Wizard

Memory Generator Wizard (for Distributed Memory)

In the 7 Series/Zynq-7000 XPE spreadsheet, the Memory Generator wizard allows you to enter distributed memory information in the Logic sheet. You can access the Memory Generator Wizard by clicking the **Manage IP** button on the IP Manager sheet or the **Add Memory** button on the Logic sheet. The XPE Memory Generator wizard provides a simplified method of populating the Logic sheet with rows related to distributed memory.

To understand the capabilities of the 7 series/Zynq-7000 distributed memory and the settings you will enter within XPE refer to the *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5].

To populate the 7 Series/Zynq-7000 Logic sheet using the XPE Memory Generator Wizard:

1. Open the Memory Generator wizard by doing one of the following:
   - On the Logic Sheet, click the **Add Memory** button.

     OR
   - On the IP Manager Sheet:
     a. Click the **Manage IP** button.

     b. In the IP Manager dialog box, select the **Create IP** tab.
     c. In the dialog box IP Catalog, select **Distributed Memory**.
     d. In the dialog box, click the **Create** button.
2. In the Distributed Memory tab of the XPE Memory Generator dialog box, fill out the information in the dialog box for one distributed memory **Memory Type** in your design.

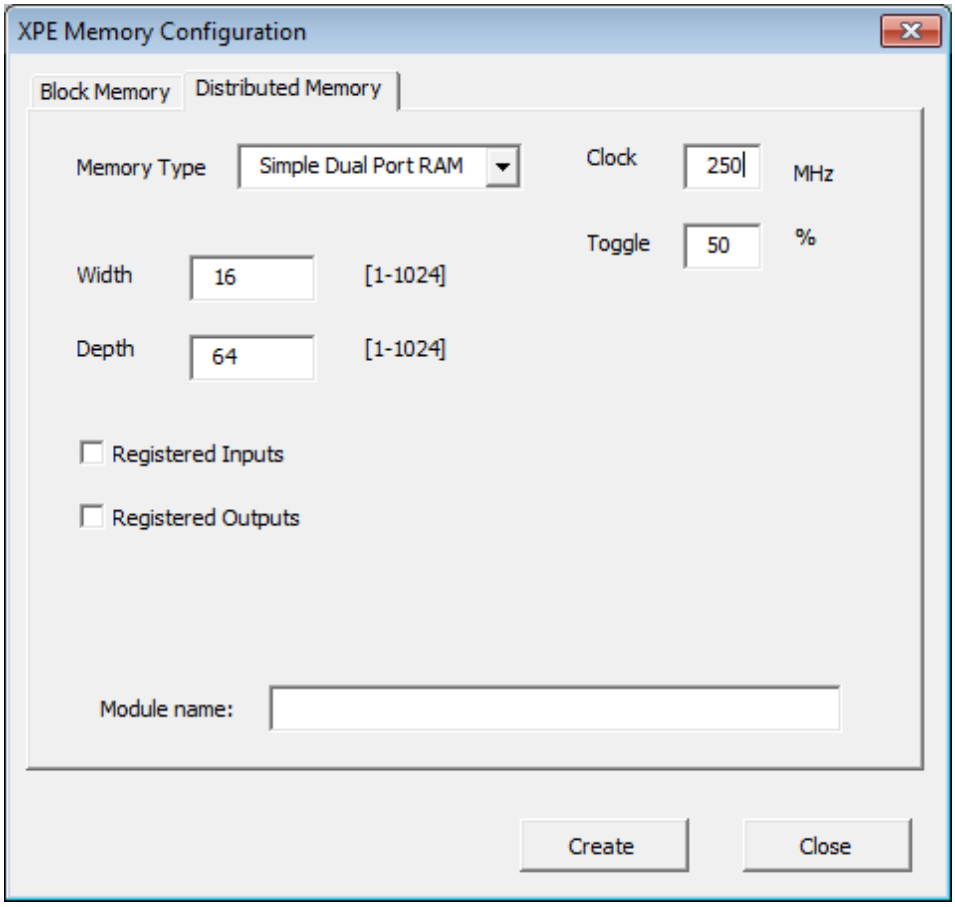


Figure 11: **Distributed Memory Tab - XPE Memory Generator Dialog Box (Virtex-7)**

The fields in the Distributed Memory tab are:

- **Memory Type**

  Select the type of memory your design will use.

  - **Single Port RAM**
  - **Simple Dual Port RAM**
  - **Single Port ROM**
  - **Dual Port ROM**

  For a description of these memory types, see the *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5].

- **Clock**

  Enter the clock frequency at which the distributed memory will operate.

  For dual-port memory types, XPE assumes the same clock frequency for both ports.

- **Toggle**

  Enter the average toggle rate of the data signals. A toggle rate of 50% means that half of the data signals toggle each clock cycle.

- **Width**

  Enter the bit width for each word in the memory.

- **Depth**

  Enter the depth of the memory. **Width** × **Depth** is the total number of bits in the memory.

- **Registered Inputs**

  Specify whether the memory inputs will be registered (**Registered Inputs** selected) or not (**Registered Inputs** deselected).

  For a description of input registering, see the *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5].

- **Registered Outputs**

  Specify whether the memory outputs will be registered (**Registered Outputs** selected) or not (**Registered Outputs** deselected).

  For a description of output registering, see the *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5].

- **Module name**

  Allows you to assign a name to the generated distributed memory configuration. This will help to distinguish multiple configurations in the XPE sheets.

3. When you have filled out the values for this distributed memory, click **Create**.

   A row in the Logic sheet will be filled in with the information you entered in the dialog box.

4. For each distributed memory type in your design, fill out the dialog box and click **Create**.

   Each time you click **Create** a row will be added to the Logic sheet.

5. When you have configured all of the distributed memory in your design, click **Close** to close the XPE Memory Generator dialog box.

Memory Generator Wizard (for Block Memory)

In the 7 Series/Zynq-7000 XPE spreadsheet, the Memory Generator wizard allows you to enter block memory information in the spreadsheet. You can access the Memory Generator Wizard by clicking the **Manage IP** button on the IP Manager sheet or the **Add Memory** button on the Block RAM sheet. The XPE Memory Generator wizard provides a simplified method of filling in the Block RAM sheet in XPE.

To understand the capabilities of the 7 series block memory and the settings you will enter within XPE refer to the 7 Series FPGAs Memory Resources User Guide (UG473) .

To populate the 7 Series Block RAM sheet using the XPE Memory Generator Wizard:

1. Open the Memory Generator wizard by doing one of the following:
   - On the Block RAM sheet, click the **Add Memory** button.

     OR
   - On the IP Manager Sheet:
     a. Click the **Manage IP** button.

     b. In the IP Manager dialog box, select the **Create IP** tab.
     c. In the dialog box IP Catalog, select **Block Memory**.
     d. In the dialog box, click the **Create** button.
2. In the Block Memory tab of the XPE Memory Generator dialog box, fill out the information in the dialog box for one block memory **Memory Type** in your design.

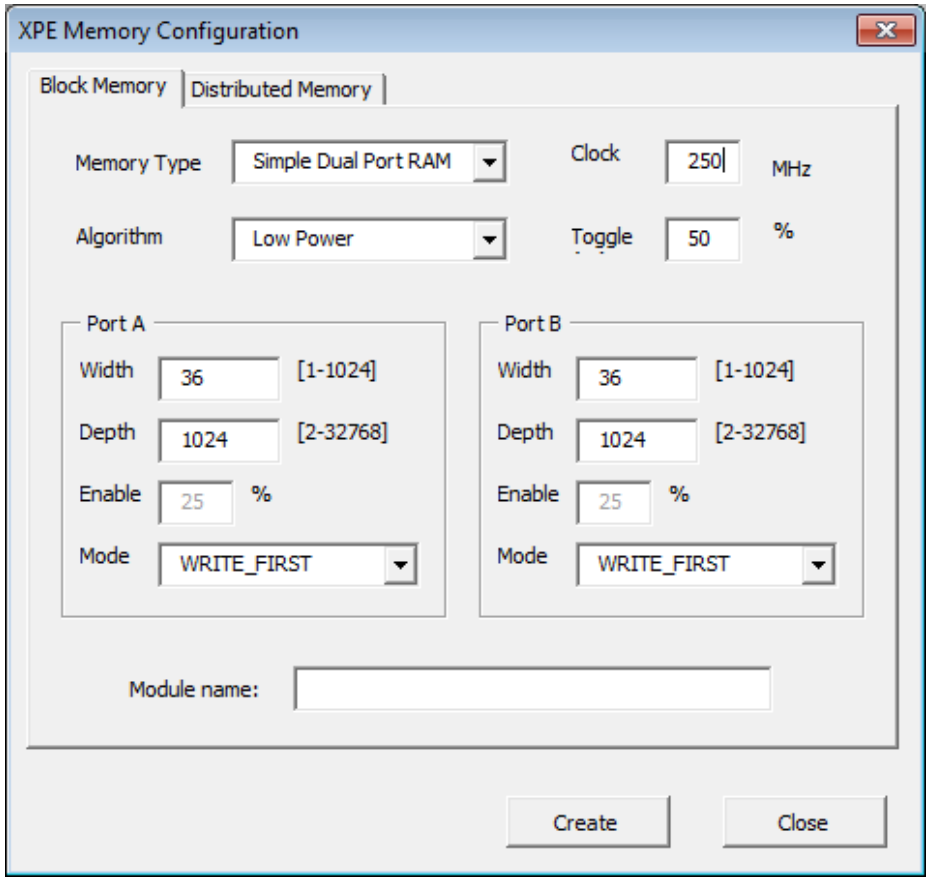


Figure 14: **Block Memory Tab - XPE Memory Generator Dialog Box (Virtex-7)**

The fields in the Block Memory tab are:

- **Memory Type**

  Select the type of memory your design will use.

  - **Single Port RAM**
  - **Simple Dual Port RAM**
  - **True Dual Port RAM**
  - **Single Port ROM**
  - **Dual Port ROM**

  For a description of these memory types, see the *7 Series FPGAs Memory Resources User Guide (UG473)* [Ref 6].

- **Clock**

  Enter the clock frequency at which the block RAM will operate.

  For dual-port memory types, XPE will assume the same clock frequency for both **Port A** and **Port B**.

- **Algorithm**

  Specify which of these algorithms the Xilinx design tools will use to configure block RAM primitives and connect them together:

  - **Minimum Area**

    The memory is generated using the minimum number of block RAM primitives.

  - **Low Power**

    The memory is generated such that the minimum number of block RAM primitives are enabled during a Read or Write operation.

- **Toggle**

  Enter the average toggle rate of the data signals. A toggle rate of 50% means that half of the data signals toggle each clock cycle.

- **Port A** and **Port B**

  If you have selected a single port **Memory Type**, you will enter information for **Port A** only. If you have selected a dual port **Memory Type**, you will enter information for both **Port A** and **Port B**.

  - **Width**

    Enter the bit width for each word in the port.

  - **Depth**

    Enter the depth of the port. **Width** × **Depth** is the total number of bits in the memory.

  - **Enable**

    Enter the percentage of time that the port will be enabled.

  - **Mode**

    Select the operating mode for the block RAM: **READ_FIRST**, **WRITE_FIRST**, or **NO_CHANGE**.

    For a description of these modes, see the *7 Series FPGAs Memory Resources User Guide (UG473)* [Ref 6].

- **Module name**

  Allows you to assign a name to the generated block memory configuration. This will help to distinguish multiple configurations in the XPE worksheets.

3. When you have filled out the values for this block memory, click **Create**.

   A row in the Block Ram sheet and a row in the Logic sheet will be filled in with the information you entered in the dialog box.

4. For each block memory type in your design, fill out the dialog box and click **Create**.

   Each time you click **Create** a row is added to the Block RAM sheet and the Logic sheet.

5. When you have configured all of the block memory in your design, click **Close** to close the XPE Memory Generator dialog box.

Memory Interface Configuration Wizard

For the 7 Series XPE spreadsheet, you can enter information for the I/Os involved in the interface between the FPGA and external memory by using the Memory Interface Configuration wizard. The Memory Interface Configuration wizard provides a simplified method of filling in the memory interface I/Os in the XPE spreadsheet.

When you configure a memory interface using the wizard, rows will be added to the I/O sheet for each output line (for example, Data, Address, and Clock) from the FPGA that will be applied to the external memory. The wizard will also place rows on the Clock sheet and on the sheet for any clock manager (for example, PLL or MMCM) that is part of the memory interface.

The Memory Interface Configuration wizard does not support all memory interface standards or all interface parameters for the supported standards. The wizard covers many of the common Memory Interface Standards. For a specific standard there could be more pins associated than configured by the wizard. In these cases you may need to modify the output of the wizard or enter the extra pins manually in the I/O sheet for your specific case. Also, if a selection is not available for a specific field, you may be able to manually override the selections in the field.

To understand the 7 series memory interfaces and the settings you will enter within XPE refer to the *7 Series FPGAs Memory Interface Solutions User Guide (UG586)* [Ref 9].

To add memory interface I/Os to the 7 series I/O sheet using the Memory Interface Configuration Wizard:

1. Open the Memory Interface Configuration wizard by doing one of the following:
   - On the I/O sheet, click the **Add Memory Interface** button.

   OR

   - On the IP Manager Sheet:
     a. Click the **Manage IP** button.

     b. In the IP Manager dialog box, select the **Create IP** tab.
     c. In the dialog box IP Catalog, select **Memory Interface**.
     d. In the dialog box, click the **Create** button.
2. In the XPE Memory Interface Configuration dialog box, fill out the information in the dialog box for one memory interface in your design.

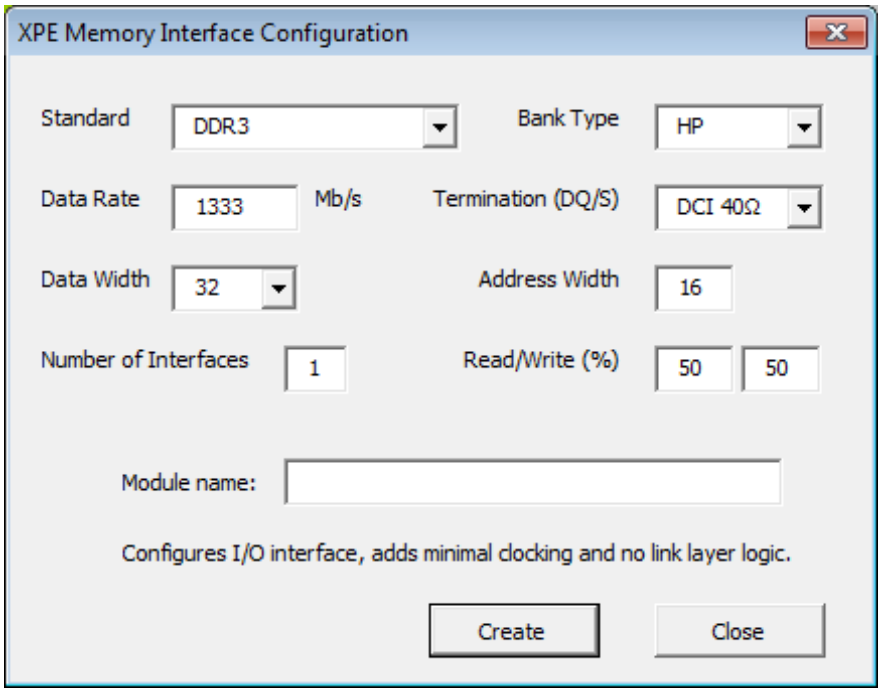


Figure 17: **XPE Memory Interface Configuration Dialog Box (Virtex-7)**

The fields in the XPE Memory Interface Configuration dialog box are:

- **Standard**

  The Memory Interface Configuration wizard supports these I/O Standards:

  - DDR2
  - DDR3
  - DDR3L
  - QDR2+
  - RLDRAM2
  - RLDRAM3
  - LPDDR2

  You can also manually enter a memory interface of any other standard in the XPE spreadsheet.

  For a listing of the supported I/O standards and limits for your specific device, see the appropriate data sheet:

  - *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics (DS183)* [Ref 10]
  - *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics (DS182)* [Ref 11]
  - *Artix-7 FPGAs Data Sheet: DC and Switching Characteristics (DS181)* [Ref 12]

- **Bank Type**

  Select the appropriate **Bank Type**, where the choice exists.

- **Data Rate**

  Enter the target **Data Rate** for your memory device.

- **Termination (DQ/S)**

  Refers to the DQ (data) and DQS (data strobe) pins. For memory interfaces using the HP banks DCI termination is used as appropriate depending on the **Standard** selected. For the HR banks **INTERM_40**, **INTERM_50**, **INTERM_60** or external termination (no entry) may be selected.

- **Data Width**

  Values from 8-144 in increments of 8 are supported, with memory type and device restrictions. Address, data, and control signals must be in the same I/O column so the limit is often lower than 144. Stacked Silicon Interconnect (SSI) technology devices are limited to a width of 72 due to this restriction.

- **Address Width**

  The total number of address lines used in the interface, which includes Row, Col, Bank, and, if used, Rank and CS lines.

- **Number of Interfaces**

  Enter the number of memory interfaces that will use the settings that you are currently entering in the dialog box. When the I/O sheet is populated with the outputs to external memory, the number of pins for each type of line (for example, Address, Data, and Clock lines) will reflect the number of **Interfaces** you specify.

- **Read/Write (%)**

  Specifies the percentage of the time the memory interface is used for reading from and writing to the external memory. The total must be less than or equal to 100% and the interface is assumed to be idle for 100% - (Read% + Write%) of the time. This is reflected in the **Output Enable**, **Term Disable** and **IBUF Disable** percentages.

- **Module Name**

  Allows you to assign a name to the generated configuration. This will help to distinguish multiple configurations on the I/O sheet.

3. When you have filled out the values for this memory interface, click **Create**.

   Rows in the I/O sheet will be populated with the information you entered in the dialog box.

4. For each memory interface in your design, fill out the information in the XPE Memory Interface Configuration dialog box and click **Create**.

   Each time you click **Create** rows will be added to the I/O sheet.

5. When you have configured all of the memory interfaces in your design, click **Close** to close the XPE Memory Interface Configuration dialog box.

Transceiver Configuration Wizard

For the 7 Series XPE spreadsheet, you can enter transceiver information in an MGT sheet (GTP, GTH, GTX, or GTZ) by using the Transceiver Configuration wizard. The Transceiver Configuration wizard provides a simplified method of filling in the MGT sheets in the XPE spreadsheet.

IMPORTANT: *The Transceiver Configuration wizard does not support all transceiver protocols or all transceiver parameters for the supported protocols. Any options not available in a dialog box field need to be entered manually in the field. Any cases where a quad has transceivers using both CPLL and QPLL, different transmit and receive rates, or different power modes, will also have to be entered manually. The wizard covers many common protocols, but you may need to modify the output of the wizard or enter the data manually in the MGT sheet for your specific case.*

To understand the capabilities of the 7 series MGTs and the settings you will enter within XPE refer to the *7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7] and the *7 Series FPGAs GTP Transceivers User Guide (UG482)* [Ref 8].

To populate the 7 Series MGT sheet using the XPE Transceiver Configuration Wizard:

1. Open the Transceiver Configuration wizard by doing one of the following:
   - On the applicable MGT sheet, click the **Add GT Interface** button (sample shown below).

     OR
   - On the IP Manager Sheet:
     a. Click the **Manage IP** button.

     b. In the IP Manager dialog box, select the **Create IP** tab.
     c. In the dialog box IP Catalog, select **Transceiver Interface**.
     d. In the dialog box, click the **Create** button.
2. In the XPE Transceivers Configuration dialog box, fill out the information in the dialog box for one set of transceivers in your design.

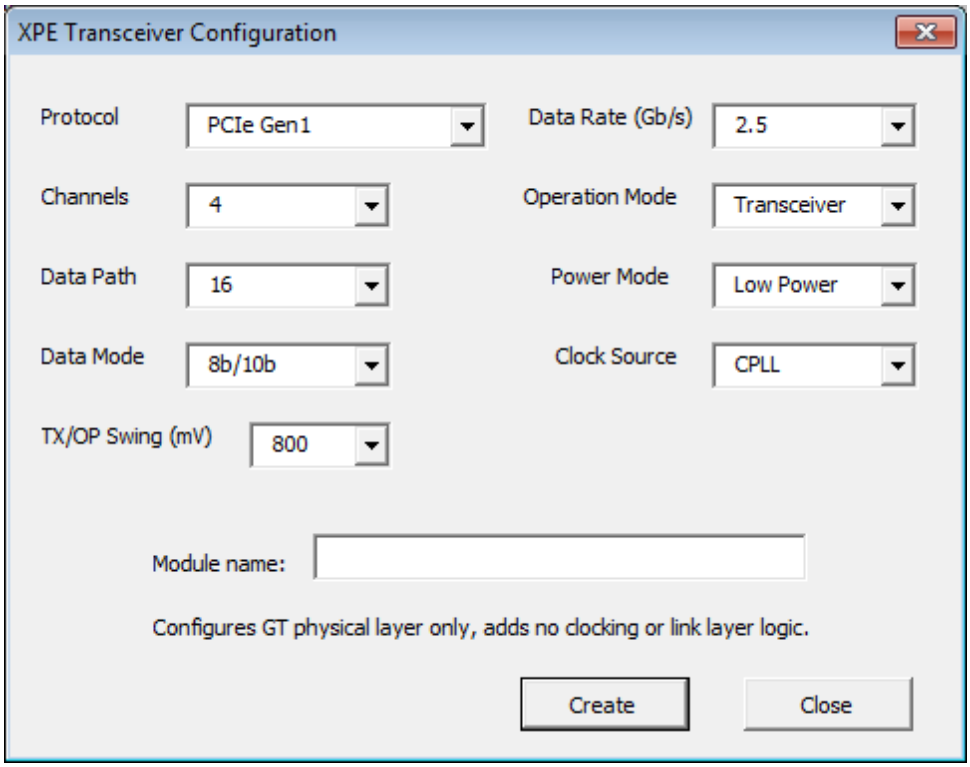


Figure 20: **XPE Transceiver Configuration Dialog Box (Virtex-7)**

The fields in the XPE Transceivers Configuration dialog box are:

- **Protocol**

  Allows you to select from a list of available protocols. Device, package, and speed grade limitations will limit the choices available. In some cases the number of **Channels**, **Data Mode** and **Clock Source** selections will default to values defined by the **Protocol**. The GTP configuration will not have **Power Mode** or **Clock Source** selections. The **Data Rate** and number of **Channels** will also be reflected in the PCIe information (on a GTX, GTP, or GTH sheet) as appropriate. No clocks or fabric are populated in their respective sheets.

- **Data Rate**

  After selecting the **Protocol** the **Data Rate** will either display as a fixed value defined by the **Protocol** or allow you to enter the specific **Data Rate** used in your system. Except for the rare cases where receive and transmit rates are different, both RX and TX rates will match.

- **Channels**

  Some protocols (for example, PCIe) have specific restrictions for the number of channels and others allow you to enter the number of channels used in your system.

- **Operation Mode**

  By default the **Transceiver** configuration is used, but you can select **Transmitter** or **Receiver** only operation.

- **Fabric Width** and **Data Mode**

  The width of the port can be configured to be two, four, or eight bytes wide. With **8b/10b** encoding used the port widths can be 16, 32 or 64 bits. With **64b/66b** encoding used the port width must be 64 bits. In **Raw** mode the port widths can be 16, 20, 32, 40, 64, or 80 bits.

- **Power Mode**

  Where the choice exists (as defined by the target transceiver) you can choose to use the power-efficient adaptive linear equalizer mode called the **Low Power** mode (LPM) or the high-performance, adaptive decision feedback equalization (**DFE**) mode.

  For a description of these modes, see the RX Equalizer (DFE and LPM) section in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 7].

- **Clock Source**

  Where the choice exists (as defined by the target device and data rate) you can choose to use the LC tank (**QPLL**) or ring oscillator (**CPLL**) based PLL.

- **Module name**

  Allows you to assign a name to the generated configuration. This will help to distinguish multiple configurations in the XPE worksheets.

3. When you have filled out the values for this set of transceivers, click **Create**.

   A row in the MGT Sheet will be filled in with the information you entered in the dialog box.

4. For each set of transceivers in your design, fill out the dialog box and click **Create**.

   Each time you click **Create** a row will be added to the MGT sheet.

5. When you have configured all of the transceivers in your design, click **Close** to close the XPE Transceivers Configuration dialog box.

Summary Sheet

The Summary sheet is the default sheet on launch and allows you to enter all device and environment settings. On this sheet the tool also reports estimated power rail-wise and block-wise so you can quickly review thermal and supply power distribution for your design (see Figure 21).

You can ad a description, short details about the design, or calculations related to the design in the following places:

- A **Project** field at the top of the Summary sheet allows you to add a description of the design.
- In the 7 Series/Zynq-7000 spreadsheet, an area of boxes to the right of the Summary sheet allows you to add a description, details about the design, or calculations related to the design. In this area you can add links, data tables, graphics, or any other object you can enter in a regular Excel document.
- In spreadsheets for pre-7 series devices, a **Comment** field at the bottom of the Summary sheet allows you to add a description or short details about the design.
- If your data does not fit in the boxes on the Summary sheet, go to the **User** sheet. There you can add links, data tables, graphics, or any other object you can enter in a regular Excel document.

TIP: *The Spartan-3, Spartan-3E and Virtex-4 spreadsheets have a slightly different layout for this sheet. The description of the different user settings and data presented in this view is, however, applicable to these spreadsheets.*

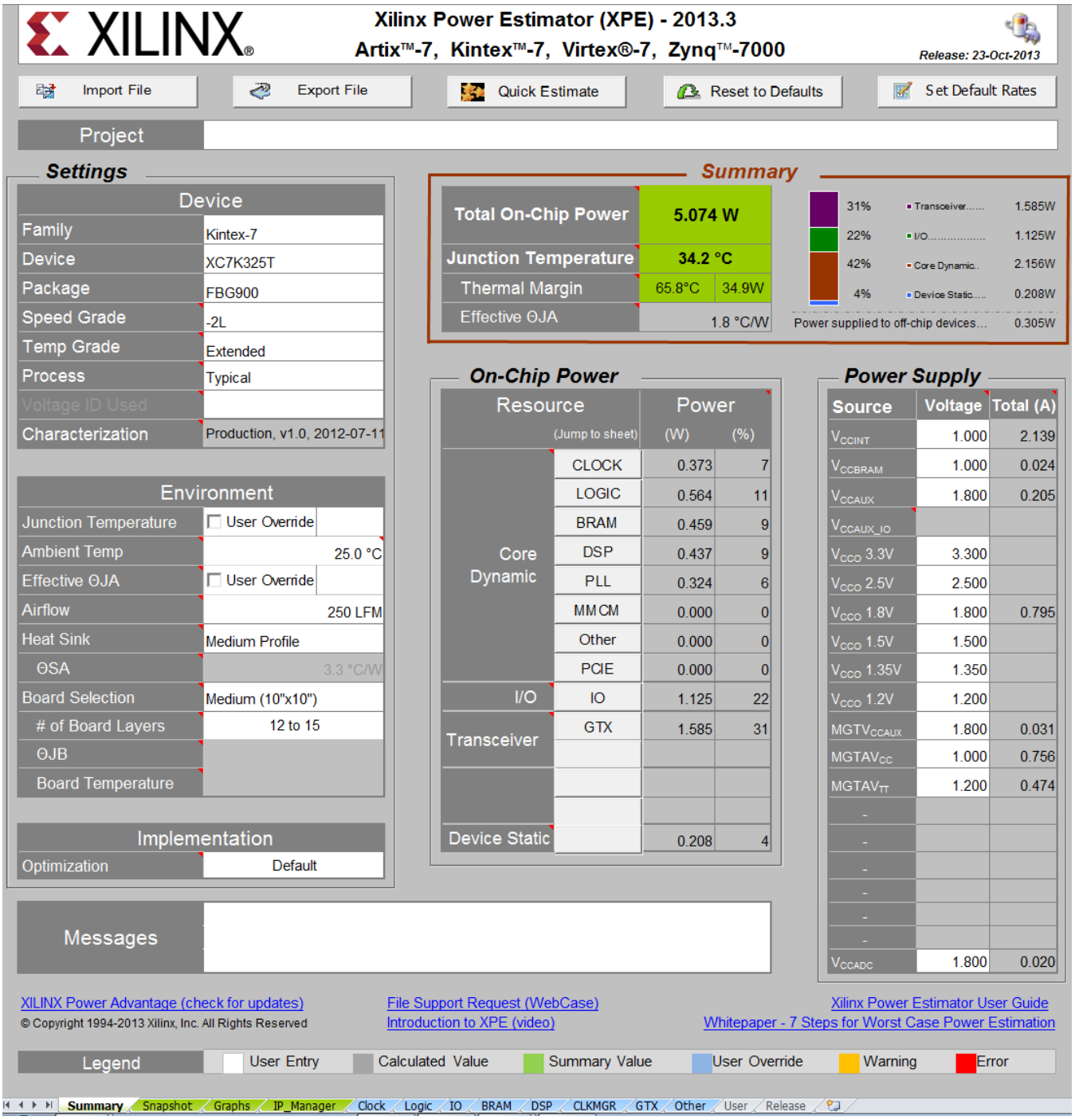


Figure 21: **Summary Sheet (Kintex-7) - Adjust Settings and Display Power Results**

Settings Panel

Use the **Settings** panel to specify details of the device, board, cooling and ISE or Vivado Design Suite settings. This panel varies slightly depending on the targeted device. A Virtex-6 example is presented in Figure 22.

Some settings are dependent on other settings. When this occurs the dependent cell becomes un-editable and turns to a grey background.

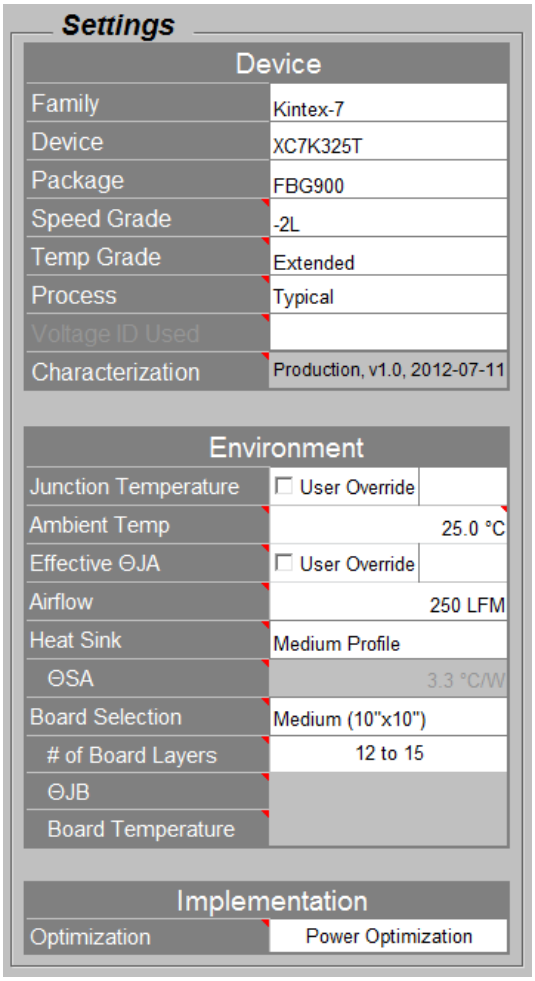


Figure 22: **Settings Panel (Kintex-7)**

The sections in the **Settings** panel are:

- **Device**

  Select the smallest device which meets your requirements.

IMPORTANT: *Larger devices exhibit higher device static power consumption.*

The 7 series spreadsheet has a **Voltage ID Used** entry, which applies to Virtex®-7, -1 **Speed Grade**, Commercial **Temp Grade**, and Maximum **Process** FPGAs only. If **Voltage ID Used** is set to Yes, XPE will perform all of its power calculations based on the device

operating at the Voltage ID voltage. The Voltage ID (VID) voltage is the minimum possible V_{CCINT} voltage at which the FPGA can run and still meet its performance specifications. This voltage is tested when the FPGA is manufactured and the value is programmed into the DNA eFuse register on the FPGA. Activating the VID feature in your design to operate the FPGA at this VID voltage can result in a significant power savings over operating the FPGA at its nominal voltage.

- **Environment**

  For XPE to report the estimated junction temperature it needs to understand how the device logic is configured and activated. It also needs a description of the device environment. The information of how heat can be transferred into the surrounding air (**ΘSA**) or PCB (**ΘJB**) affects the device junction temperature. If these parameters are known enter them; otherwise, select from the different drop-down menus the environment settings closest to your specific project. This will help to indirectly determine **Effective ΘJA**.

  For more details about the thermal parameters of the Xilinx Power Estimator, please refer to Chapter 3: Thermal Management & Thermal Characterization Methods & Conditions in the *Device Package User Guide (UG112)* [Ref 14].

- Design optimization options available in Vivado and ISE implementation

  This section is labeled:

  - **Implementation** (7 series)
  - **PL Implementation** (Zynq-7000)
  - **ISE** (earlier FPGA architectures)

  Settings in this section are available to focus the synthesis and implementation tools on minimizing towards different objectives. Adjust this area to best match the ISE or Vivado Design Suite settings you plan on using. This option affects the core dynamic power by an amount seen in a suite of customer designs.

  Optimization settings are:

  - Area Reduction – Minimize slice usage
  - Balanced – Default ISE Design Suite options
  - Default – Default ISE or Vivado Design Suite options
  - Minimum Runtime
  - Power Optimization – Minimize core dynamic power
  - Timing Performance
  - Powered Off (Zynq-7000 only)

  These options are described in the ISE Design Suite documentation for Design Goals and Strategies.

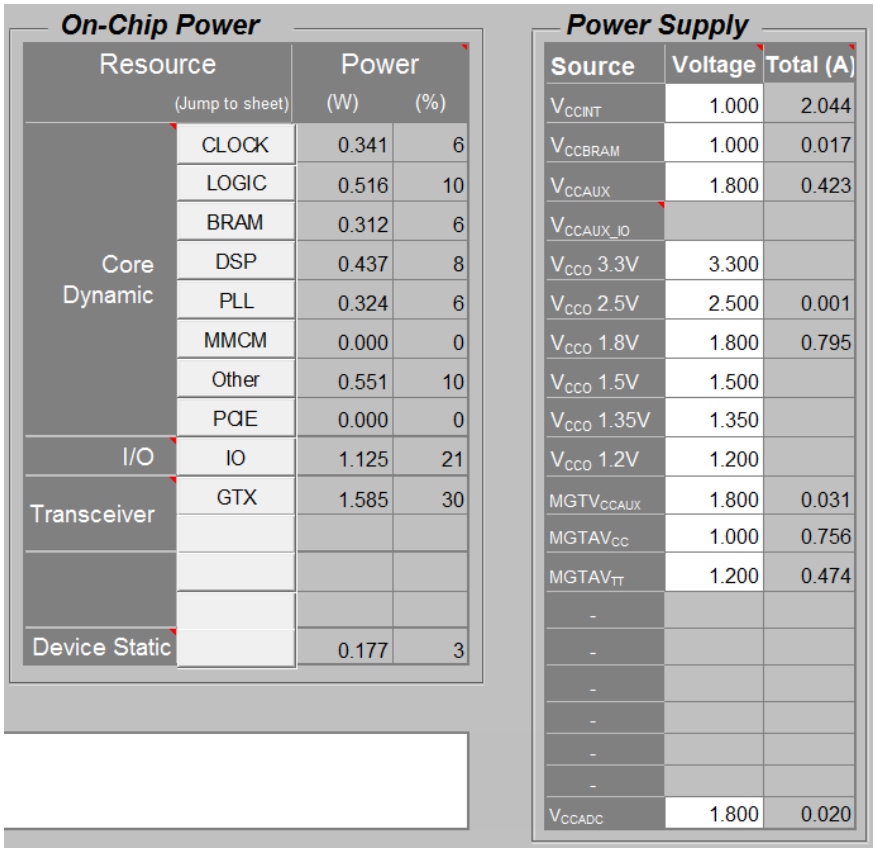
TIP: *In a 7 series spreadsheet, this section is labeled **Implementation**, and only Default and Power Optimization settings are available. In a Zynq-7000 spreadsheet, this section is labeled **PL Implementation**, and Default, Power Optimization, and Powered Off settings are available.*

- **Power mode**

  This setting allows you to review the estimated power for the different active and power down modes of the device. **Power Mode** is available for some device families.

Power Distribution Panels

There are two separate aspects to evaluate when integrating Xilinx FPGAs in a system. Typically designers first evaluate the FPGA current drawn on each voltage supply to ensure all voltage sources can provide enough power for the device to function properly. Second, designers need to know how much of that supplied power is consumed by the device itself as opposed to power supplied to off-chip components such as board termination networks. The power consumed on-chip, also referred to as thermal power, generates heat which must be transferred to the environment in order to maintain the device junction temperature within the normal operating range. Figure 23 shows the on-chip power contributing to junction temperature (**On-Chip Power** panel) and the total supply power (**Power Supply** panel).



On-Chip Power

Resource	(Jump to sheet)	Power (W)	Power (%)
Core Dynamic	CLOCK	0.341	6
	LOGIC	0.516	10
	BRAM	0.312	6
	DSP	0.437	8
	PLL	0.324	6
	MMCM	0.000	0
	Other	0.551	10
	PCIE	0.000	0
I/O	IO	1.125	21
Transceiver	GTX	1.585	30
Device Static		0.177	3

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	1.000	2.044
V_{CCBRAM}	1.000	0.017
V_{CCAUX}	1.800	0.423
V_{CCAUX_IO}		
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	0.001
V_{CCO} 1.8V	1.800	0.795
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
$MGTV_{CCAUX}$	1.800	0.031
$MGTAV_{CC}$	1.000	0.756
$MGTAV_{TT}$	1.200	0.474
-		
-		
-		
-		
-		
-		
V_{CCADC}	1.800	0.020

Figure 23: **Power Distribution Panels (7 Series)**

On-Chip Power Panel

The **On-Chip Power** panel presents the total power consumed within the device. It includes device static and user design dependent static and dynamic power. The total is broken out by resource type. This view can help determine the amount of power being consumed and dissipated by the device. It also helps identify potential areas in the user logic where trade-offs or power optimization techniques could be used to meet the targeted power budget.

In this view you can click on the resource name to directly jump to the detailed sheet for this resource.

For design static power calculations, XPE starts by assuming a blank bitstream. To "instantiate" design elements for the design static power calculations, you must enter the appropriate resource counts on the sheets with count fields and non-zero clock frequencies for the sheets without count fields. I/O termination must also be set to match the board and the design.

Power Supply Panel

The **Power Supply** panel displays the device estimated power across the different supply sources. This information can be used for instance to size or review voltage supply components, such as regulators. The table includes all power required by the internal logic along with power eventually sourced and consumed outside the FPGA, such as in external board terminations. This view includes both static and dynamic power.

You can adjust individual voltages within the supported range and XPE will calculate and display the total current required. When Maximum **Process** is selected in the **Device** table and any power-on supply current values exceed the estimated operating current requirements, the **Power Supply** panel will display the minimum power-on supply requirements, in blue. If any current values do appear in blue, the total power indicated in the **Power Supply** panel will not match the **Total On-Chip** power in the **Summary Panel**.

Multiple power supplies are required to power an FPGA. For logic resources typically available in Xilinx FPGAs, Table 3 presents the voltage source that typically powers them. This table is provided only as a guideline because these details may vary across Xilinx device families.

Table 3: **FPGA Resources and the Power Supply that Typically Powers Them**

Power Supply	Resources Powered
V_{CCINT} & **V_{CCBRAM}**(3)	• All CLB resources • All routing resources • Entire clock tree, including all clock buffers • Block RAM/FIFO • DSP slices • All input buffers • Logic elements in the IOB (ILOGIC/OLOGIC) • ISERDES/OSERDES • PowerPC™ processor(1) • Tri-Mode Ethernet MAC(1) • Clock Managers (MMCM, PLL, DCM, etc.)(1) • PCIE and PCS portion of MGTs
V_{CCO}(2)	• All output buffers • Some input buffers • Input termination • Reference resistors to DCI
V_{CCAUX} & **V_{CCAUX_IO}**(4)	• Clock Managers (MMCM, PLL, DCM, etc.)(1) • IODELAY/IDELAYCTRL • All output buffers • Differential Input buffers • V_{REF}-based, single-ended I/O standards, e.g., HSTL18_I • Phaser(1)
MGT*	• PMA circuits of transceivers

Notes:

1. These resources are available only in certain device families. Refer to the appropriate data sheets and user guides for more information.
2. V_{CCO} in bank 0 (V_{CCO_0} or V_{CCO_CONFIG}) powers all I/Os in bank 0 as well as the configuration circuitry. See the applicable *Configuration User Guide*.
3. Xilinx 7 series Block RAM/FIFO only.
4. Xilinx 7 series High Performance (HP) I/O banks only.

Summary Panel

The Summary panel presents in a concise format the main data of interest (see Figure 24).

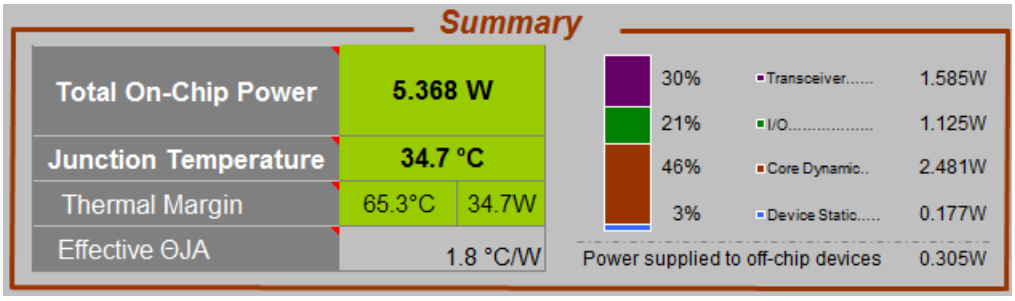


Figure 24: **Summary Panel (7 Series)**

- **Junction Temperature**

  Estimated junction temperature as the design operates. Each device operates within a temperature grade specified in the datasheet. The background for this cell turns orange when the value is outside the operating range (timing may be affected) and turns red when outside the absolute maximum temperature (device damage possible). The background color turns light blue when the value is set by user.

- **Total On-Chip Power**

  Includes power consumed and dissipated by the device across all supply sources. Also referred to as thermal power. This cell follows the color scheme of the **Junction Temperature** cell described above.

- **Thermal Margin**

  Temperature and power margin up to or in excess of the maximum accepted range for this device Grade. Thermal margin is negative when estimated junction temperature exceeds the maximum specified value. In this case, use this information to decide how best to address the excess power consumed on-chip.

- **Effective ΘJA**

  The calculated Effective Thermal Resistance (Effective ΘJA) summarizes how heat is transferred from the die to the environment. The value is calculated from the settings entered in the **Environment** panel. If you have run thermal simulations of your environment then you may also override this value (in the **Environment** panel).

Quick Estimate Wizard and the Summary Sheet

The Quick Estimate wizard populates the XPE sheets with information about your entire design, allowing XPE to perform a rough power estimate for the design. The Quick Estimate wizard is often used as the first step in specifying your design in XPE to determine its power requirements.

The Quick Estimate wizard can be started from the Summary sheet by clicking the **Quick Estimate** button.

For a description of the Quick Estimate wizard and how you can run the wizard from the Summary sheet, see Quick Estimate Wizard, page 24.

The following manuals will help you supply information to the Quick Estimate Wizard:

- *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5]
- *7 Series FPGAs Memory Resources User Guide (UG473)* [Ref 6]
- *7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7]
- *7 Series FPGAs GTP Transceivers User Guide (UG482)* [Ref 8]
- *7 Series FPGAs Memory Interface Solutions User Guide (UG586)* [Ref 9]

Power Comparison Snapshots Sheet (7 Series and Zynq-7000 Only)

The Power Comparison Snapshots sheet allows you to capture a series of snapshots of the power status of your design under varying conditions or at different points in its design cycle. Each snapshot displays device part, environmental information, the power consumed by your design, and the current across each of the power supply sources used in the design. You can use the Power Comparison Snapshots sheet to compare the power consumed under different conditions and the power calculated at different points in the design cycle.

Summary | Snapshot | Import | Clear All — Power Comparison Snapshots

Settings	Baseline	Power Optimization	Voltage ID	Industrial	2LE
	XPE: 2013.3	XPE: 2013.3	XPE: 2013.3	XPE: 2013.3	XPE: 2013.3
	8 Oct 2013 @ 17:22	8 Oct 2013 @ 17:23	8 Oct 2013 @ 17:24	8 Oct 2013 @ 17:25	8 Oct 2013 @ 17:26
	7_Series_XPE_2013_3	7_Series_XPE_2013	7_Series_XPE_2013	7_Series_XPE_2013_3	7_Series_XPE_2013_3
Part	XC7VX330TFFG1761-1C	XC7VX330TFFG1761-1C	XC7VX330TFFG1761-1C	XC7VX330TFFG1761-1I	XC7VX330TFFG1157-2LE
Ambient Temperature	68.5 °C	68.5 °C	69.9 °C	71.1 °C	71.5 °C
Process	Maximum	Maximum	Maximum	Maximum	Maximum
Implementation	Default	Power Optimization	Power Optimization+VID	Power Optimization	Power Optimization
Summary					
Total On-Chip Power	7.296 W	7.209 W	6.708 W	6.513 W	6.293 W
Junction Temperature	76.9 °C	76.8 °C	77.7 °C	78.6 °C	80.4 °C
Effective ΘJA	1.2 °C/W	1.2 °C/W	1.2 °C/W	1.2 °C/W	1.4 °C/W
On-Chip Power					
Clocking	0.697 W	0.666 W	0.666 W	0.666 W	0.666 W
Logic	0.564 W	0.516 W	0.516 W	0.516 W	0.516 W
I/O	1.640 W	1.640 W	1.640 W	1.640 W	1.640 W
BRAM	0.459 W	0.459 W	0.459 W	0.459 W	0.459 W
DSP	0.437 W	0.437 W	0.437 W	0.437 W	0.437 W
Transceiver	1.149 W	1.149 W	1.149 W	1.149 W	1.149 W
PS					
Device Static	2.350 W	2.343 W	1.841 W	1.646 W	1.427 W
Supply Summary					
V_{CCINT}	3.933 A	3.847 A	3.351 A	3.292 A	3.133 A
V_{CCBRAM}	0.099 A	0.099 A	0.099 A	0.098 A	0.097 A
V_{CCAUX}	0.629 A	0.628 A	0.633 A	0.555 A	0.523 A
V_{CCAUX_IO}					
V_{CCO} 3.3V					
V_{CCO} 2.5V	0.044 A	0.044 A	0.044 A	0.047 A	0.047 A
V_{CCO} 1.8V	0.798 A	0.798 A	0.798 A	0.801 A	0.801 A
V_{CCO} 1.5V					
V_{CCO} 1.35V					
V_{CCO} 1.2V					
$MGTV_{CCAUX}$	0.031 A	0.031 A	0.031 A	0.031 A	0.031 A
$MGTAV_{CC}$	0.603 A	0.603 A	0.604 A	0.596 A	0.592 A
$MGTAV_{TT}$	0.257 A	0.257 A	0.257 A	0.256 A	0.256 A
$MGTZV_{CCH}$					
$MGTZAV_{CC}$					
$MGTZV_{CCL}$					
V_{CCPINT}					
V_{CCPAUX}					
V_{CCPLL}					
V_{CCO_DDR}					
V_{CCO_MIO0}					
V_{CCO_MIO1}					
V_{CCADC}	0.025 A	0.025 A	0.025 A	0.025 A	0.025 A

Figure 26: **Power Comparison Snapshots Sheet (7 Series)**

A snapshot can represent:

- Power information for this XPE spreadsheet, captured at a certain time. When you create the snapshot, all of this information is copied from the Summary sheet of this spreadsheet to the Power Comparison Snapshots sheet.
- Power information for a different XPE spreadsheet, captured at a certain time. When you create the snapshot, all of this information is copied from the Summary sheet of the other spreadsheet to this Power Comparison Snapshots sheet.

- Power information for a design implemented in ISE, captured at a certain time. When you create the snapshot, the power information is imported from the ISE Power Report into the Power Comparison Snapshots sheet.

The Power Comparison Snapshots sheet allows you to explore What If? scenarios, changing the part or the environmental conditions under which the part will operate and observing the effect on power the changes will have. You can also create a snapshot of the power calculated when your design is implemented in ISE, to see how the power calculated for the implemented design compares to the power calculated before the design was implemented.

Using snapshots, you can explore What If? scenarios such as:

- How will power consumption change if I implement a design in different Xilinx architectures? What is the difference in power consumption when the same design is implemented in a Kintex device versus an Artix device?
- How does a design's power consumption vary as a function of junction temperature?
- How does a design's GT Power consumption change as a function of device type?
- How much power could be saved by using power optimization, or by choosing a -2L (low power) or a 0.9V part?
- How does the power and temperature vary under nominal versus maximum operating conditions?
- How does the design's power consumption vary as the design undergoes revision with respect to power, features, and performance?
- How does the power consumption vary between the Xilinx Power Estimator (XPE), XPower Analyzer (XPA), and Vivado Report Power estimations?
- How does the power consumption vary with changing clock frequencies?
- How did my pre-design estimate compare with post-design results and imported design data?

The four sections in the Power Comparison Snapshots sheet are:

- **Settings** - Displays the following:
  - The name of the snapshot (top line in the table)
  - Source and version of the snapshot data creator (for example, "ISE: 13.4" for an imported snapshot)
  - Data and Time the snapshot was created
  - The filename of XPE or the imported source
  - The **Part** (device, package, and speed grade) for which the power values were calculated.

- The value for **Ambient Temperature** under which the device will operate, as specified when the snapshot was taken.
- The **Process** (Typical or Maximum) specified when the snapshot was taken. The **Process** setting accounts for the power dissipation caused by the manufacturing process.
- The **Implementation** (Default or Power Optimization) specified when the snapshot was taken. This setting focuses the synthesis and implementation tools in the ISE Design Suite or the Vivado Design Suite on minimizing towards different objectives when the design is implemented.

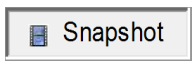
- **Summary** - Displays the following:
  - **Total On-Chip Power** - The total power consumed within the device for each snapshot. It includes device static and design dependent static and dynamic power.
  - The values for **Junction Temperature** and **Effective ΘJA** under which the device will operate, as specified when the snapshot was taken.
- **On-Chip Power** - The **On-Chip Power** section presents the total power consumed within the device by each resource type.

  In some cases, more than one resource will be included in a single row. For example, the **Clocking** row may include the power associated with clock nets as well as the power associated with clock managers such as the PLL and the MMCM, and the **Transceiver** row may include the power associated with Multi-Gigabit Transceivers (MGTs) as well as the power associated with a PCIe block.
- **Supply Summary** - Displays the estimated current across the different supply sources. The table includes all power required by the internal logic along with power eventually sourced and consumed outside the FPGA, such as in external board terminations. This view includes both static and dynamic power.

Adding a Snapshot of the Current Spreadsheet

To add a snapshot of the current XPE spreadsheet to the Power Comparison Snapshots sheet:

1. Click the **Snapshot** button on the Power Comparison Snapshots sheet.

   A snapshot for the current XPE spreadsheet appears in the far right column of the table in the sheet.
2. If desired, rename the snapshot at the top row of the table.

Importing a Snapshot

You can import a snapshot containing power values calculated from a different XPE spreadsheet or power values calculated when the design is implemented in the ISE Design Suite or the Vivado Design Suite.

Note: When you import power information into the Power Comparison Snapshots sheet, the FPGA or AP SoC device represented in the imported data does not have to match the device specified in the current XPE spreadsheet.

To import a snapshot into the Power Comparison Snapshots sheet:

1. Click the **Import** button at the top of the Power Comparison Snapshots sheet.

   A snapshot for the current XPE spreadsheet will appear in the far right column of the table in the sheet.

2. In the Select XPE File to Import dialog box, select the following in the **Files of type** box:
   - **XPE Workbook (*.xls*)**, if you are importing information from a different XPE spreadsheet.
   - **Power Report (*.pwr)**, if you are importing information from a Power Report generated within the ISE Design Suite or the Vivado Design Suite.
3. Browse to the file you will import and click **Open**.

A snapshot appears in the far right column of the table in the Power Comparison Snapshots sheet. If desired, rename the snapshot at the top row of the table.

Deleting Snapshots from the Power Comparison Snapshots Sheet

To delete a single snapshot, click the box with the red "**X**" at the top of the snapshot.

To delete all of the snapshots on the Power Comparison Snapshots sheet, click the **Clear All** button at the top of the sheet.

IP Manager Sheet (7 Series and Zynq-7000 Only)

The IP Manager sheet lets you create, view, and delete IP modules created using the IP Module wizards. You can also export IP modules (to be imported into other XPE spreadsheets), and import modules from other XPE spreadsheets into your currently active spreadsheet.

Each IP module displayed in the IP Manager sheet represents the device resources used to implement one of the following in a Xilinx device:

- Block memory - Created using the Memory Generator Wizard (for Block Memory).
- Distributed memory - Created using the Memory Generator Wizard (for Distributed Memory).
- Memory interface - Created using the Memory Interface Configuration Wizard.
- Transceiver interface - Created using the Transceiver Configuration Wizard.

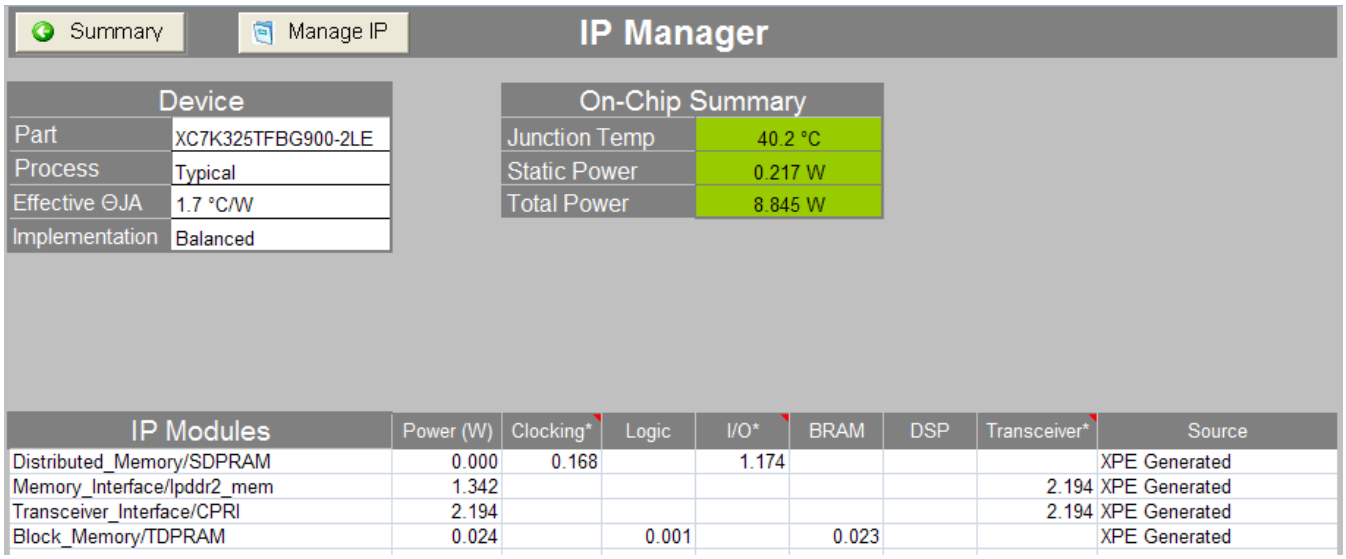


Figure 29: **IP Manager Sheet (7 Series)**

The **IP Modules** table indicates the power associated with each IP module created, as well as the power associated with the resource sheets populated by the IP module. As shown in the **IP Modules** table in **Figure 29**, IP modules may populate more than one resource sheet. For example, a block memory IP module may place rows in both the Block RAM sheet (**BRAM** column) and the Clock sheet (**Clocking** column).

n some cases, more than one resource will be included in a single column in the **IP Modules** table. For example, the **Clocking** column may include the power associated with clock nets as well as the power associated with clock managers such as the PLL and the MMCM, and the **Transceiver** column may include the power associated with Multi-Gigabit Transceivers (MGTs) as well as the power associated with a PCIe block.

Creating an IP Module From the IP Manager Sheet

For a description of how to create IP modules from the IP Manager sheet, see the following:

- Block Memory - See Memory Generator Wizard (for Block Memory), page 31.
- Distributed Memory - See Memory Generator Wizard (for Distributed Memory), page 27.
- Memory Interface - See Memory Interface Configuration Wizard, page 34.
- Transceiver Interface (7 Series only) - See Transceiver Configuration Wizard, page 38.

Deleting an IP Module From the IP Manager Sheet

To delete an IP module from the IP Manager sheet:

1. Click the **Manage IP** button at the top of the IP Manager sheet.

   The XPE IP Manager dialog box opens.

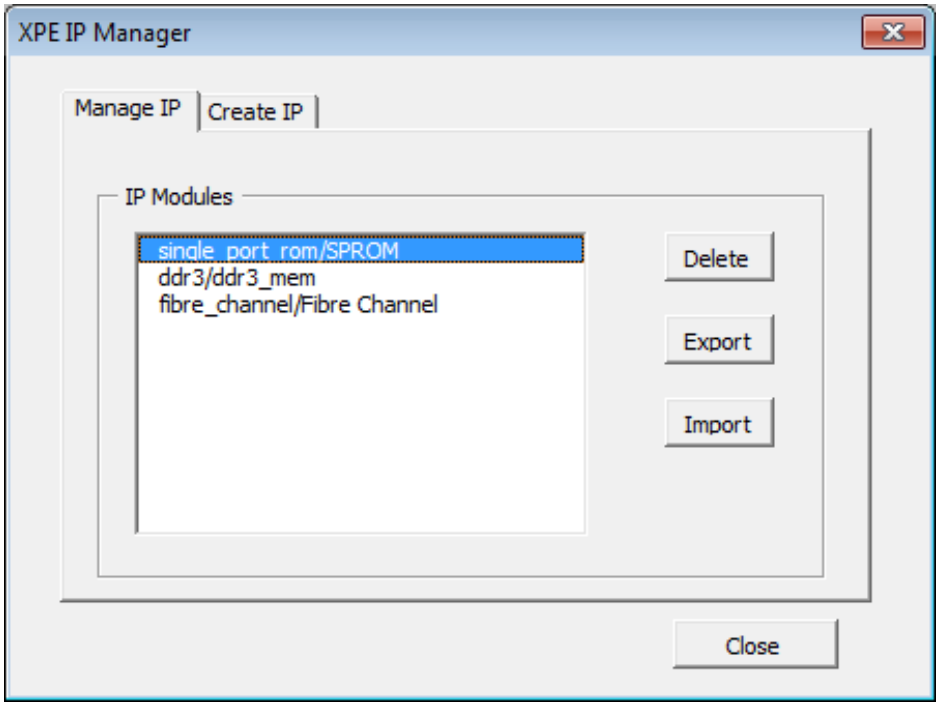


Figure 30: **XPE IP Manager Dialog Box**

2. In the Manage IP tab of the XPE IP Manager dialog box, select the IP module you want to delete and click **Delete**.

   All of the rows in the appropriate resource sheets are deleted, and the IP Module is removed from the **IP module** table on the IP Manager sheet.

Exporting an IP Module From the IP Manager Sheet

An IP module can be exported from the currently active XPE spreadsheet, for importing into another XPE spreadsheet. IP modules are exported as .xpe (XPE Exchange) files.

To export an IP module from the IP Manager sheet:

1. Click the **Manage IP** button at the top of the IP Manager sheet.

   The XPE IP Manager dialog box opens (see Figure 30).

2. In the Manage IP tab of the XPE IP Manager dialog box, select the IP module you want to export and click **Export**.
3. In the Export Xilinx Power Estimator IP Module dialog box, specify a **File name** for the .xpe file representing the selected IP module. Then click **Save**.

   The selected IP module is exported to an .xpe (XPE Exchange) file. This file can be imported into another XPE spreadsheet.

Importing an IP Module Into the IP Manager Sheet

An IP module can be imported into the IP Manager sheet. IP modules are imported as .xpe (XPE Exchange) files. The imported .xpe file represents an IP module exported from another XPE spreadsheet.

To import an IP module into the IP Manager sheet:

1. Click the **Manage IP** button at the top of the IP Manager sheet.

   he XPE IP Manager dialog box opens (see Figure 30).

2. In the Manager IP tab of the XPE IP Manager dialog box, click **Import**.
3. In the Import Xilinx Power Estimator IP Module dialog box, specify the **File name** of the .xpe file to be imported. Then click **Save**.

   The selected .xpe file is imported into the IP Manager sheet.

Resource Sheets

The following sections provide details for entering data into or interpreting results in the different available resource sheets. XPE only shows sheets available on the particular FPGA family and device selected. These resource sheets are organized with a center table where you enter utilization, configuration, and activity of the device resources you use. Above this main table are tables representing the total utilization and a summary of the resource's contribution to the total power per voltage supply.

These sheets represent usage based power; therefore, they include all power related to the utilization and configuration of the specified resource. The sheets do not include the leakage power contribution, since this is accounted for on the Summary sheet.

RECOMMENDED: *On sheets in which you specify a clock frequency for resources, XPE will assume that all resources on a single row in the sheet (for example, 4000 Shift Registers and 3000 FFs in a single row on the Logic sheet) are in the same clock domain. For an accurate power estimation, make sure to enter resources in different clock domains on separate rows in the spreadsheet.*

Clock Sheet

Important factors in dynamic power calculation are the activity and the load capacitance that needs to be switched by each net in the design. Some of the factors in determining the loading capacitance are fanout, wire length, etc. With clocks typically having higher activity and fanouts, the power associated with clock nets can be significant and thus is reported in a separate worksheet sheet (see Figure 31).

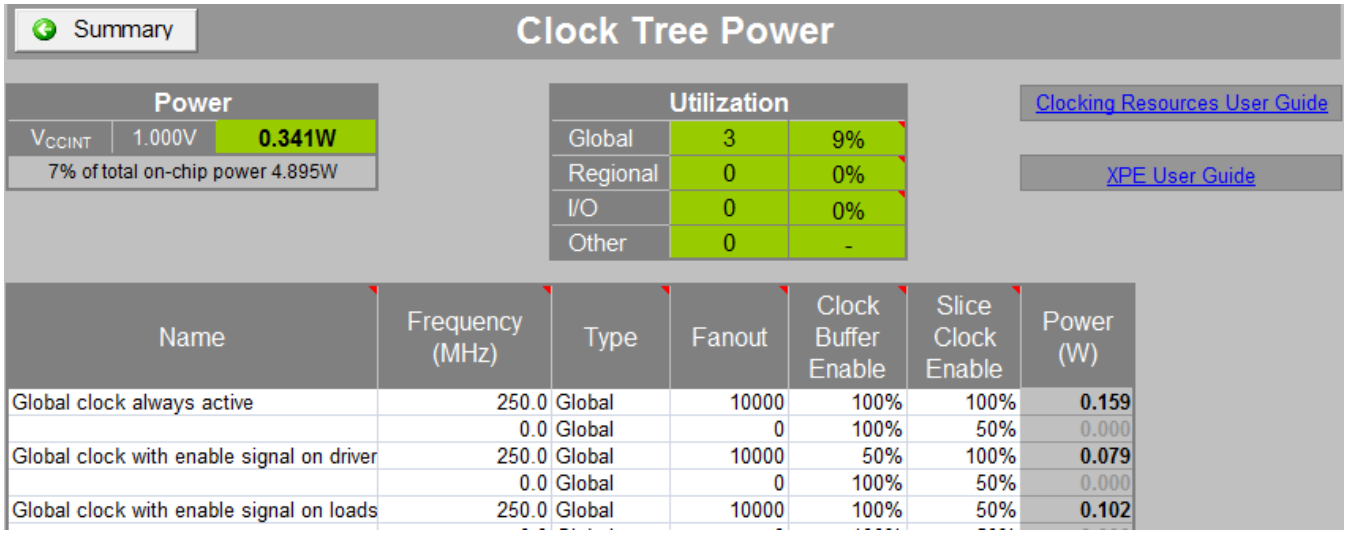


Figure 31: **Clock Tree Power Sheet (7 Series)**

- Buffer **Type** Column

  Xilinx devices have different types of buffers capable of driving the clock routing structures and these types are modeled within XPE. Refer to the applicable *Device User Guide* to select the appropriate buffer type.

- Clock **Fanout** Column

  The number of synchronous elements driven by this clock.

- **Clock Buffer Enable** Column

  Gates the clock net at its source. The value is the percentage of the time in which the clock buffer is active. Reduce this percentage if you plan on disabling the clock net at the source when this portion of the design is not used. This reduces power.

- **Slice Clock Enable** Column

  Gates the clock net at its loads. Reduce this percentage if you plan on disabling some of the clock loads with slice level Clock Enable signals. This reduces power.

  Note: Some algorithms in software such as "Intelligent Clock Gating" will remap or change the packing in order to minimize this number.

Logic Sheet

The Logic sheet (see Figure 32) is used to estimate the power consumed in the CLB resources. The estimated power accounts for both the logic components and the routing. Two types of information should be entered:

- **Utilization** – Enter the number of LUTs configured as Logic, Shift Registers and LUT-based RAMs and ROMs. If your design or a previous generation has been implemented within ISE or the the Vivado Design Suite use the **Import** button in the Summary sheet to automatically import this information. Otherwise, use your experience to estimate utilization required to implement the desired functionality.
- **Activity** – Enter the **Clock** domain this logic belongs to. Then enter the **Toggle Rate** the logic is expected to switch and the **Average Fanout**.

TIP: *The default setting for **Toggle Rate** (12.5%) and **Average Fanout** (3) are based on an average extracted from a suite of customer designs. In the absence of a better estimate for your specific design, Xilinx recommends using the default setting.*

Note: The **Signal Rate** column defines the number of millions of transitions per second for the considered element. This is a read-only column.

Signal Rate is computed in this way:

Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Toggle rate (%)

Summary | Add Memory | Logic Power

Power		
V_{CCINT}	1.000V	0.582W
12% of total on-chip power 4.895W		

Utilization		
Registers	20,000	5%
LUTs	48,000	24%
Combinatorial	40,000	20%
Shift Registers	1,000	6%
Distributed RAMs	7,000	

CLB User Guide

XPE User Guide

Name	Clock (MHz)	LUTs as Logic	LUTs as Shift Registers	LUTs as Distributed RAMs	Registers	Toggle Rate	Average Fanout	Signal Rate (Mtr/s)	Power (W)
LUTs	250.0	20000	0	0	0	12.5%	3.00	31.3	0.139
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
LUTs with high fanout	250.0	20000	0	0	0	12.5%	6.00	31.3	0.184
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Registers	250.0	0	0	0	10000	12.5%	3.00	31.3	0.050
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Registers with high activity	250.0	0	0	0	10000	25.0%	3.00	62.5	0.099
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Shift registers	250.0	0	1000	0	0	12.5%	3.00	31.3	0.020
	0.0	0	0		0	12.5%	3.00	0.0	0.000
Distributed memory	250.0	0	0	7000	0	12.5%	3.00	31.3	0.089
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000

Figure 32: **Effect of LUT Configuration, Toggle Rates and Average Fanout on Power Estimation (7 Series)**

To enter information on the Logic sheet related to distributed memory, you can use the XPE Memory Generator wizard, which appears when you click the **Add Memory** button on the Logic sheet. The XPE Memory Generator wizard provides a simplified method of adding memory-related rows to the Logic sheet. For information about using this wizard, see Memory Generator Wizard and the Logic Sheet (Distributed Memory), page 60.

Memory Generator Wizard and the Logic Sheet (Distributed Memory)

For the 7 series/Zynq-7000 XPE spreadsheet, you can enter distributed memory information in the Logic sheet by using the Memory Generator wizard. The Memory Generator wizard provides a simplified method of populating the Logic sheet with rows related to distributed memory, displayed as **Distributed RAMs** on the Logic sheet.

The Memory Generator wizard can be started from the Logic sheet by clicking the **Add Memory** button.

For a description of the Memory Generator wizard and how you can run the wizard from the Logic sheet, see Memory Generator Wizard (for Distributed Memory), page 27.

To understand the capabilities of the 7 series/Zynq-7000 distributed memory and the settings you will enter within XPE refer to the *7 Series FPGAs Configurable Logic Block User Guide (UG474)* [Ref 5].

I/O Sheet

With higher switching speeds and capacitive loads, switching I/O power can be a substantial part of the total power consumption of an FPGA. Because of this, it is important to accurately define all I/O related parameters. In the I/O sheet XPE helps you calculate the on-chip and, eventually, off-chip power for your I/O interfaces.

For 7 series devices, XPE provides a Memory Interface Configuration wizard to allow you to quickly enter the important parameters required for an accurate power estimate of the I/Os involved in the FPGA's interface to external memory. For step-by-step instructions about how to use the wizard to fill out the memory interface information in the I/O sheet, see Memory Interface Configuration Wizard and the I/O Sheet, page 66.

Figure 34 shows the top section of the I/O sheet (for the 7 series spreadsheet). Note that this sheet, as well as other sheets in the 7 series spreadsheet, contains a button to display applicable documentation from the Xilinx website (in this case, the *7 Series FPGAs SelectIO Resources User Guide (UG471)* [Ref 15]).

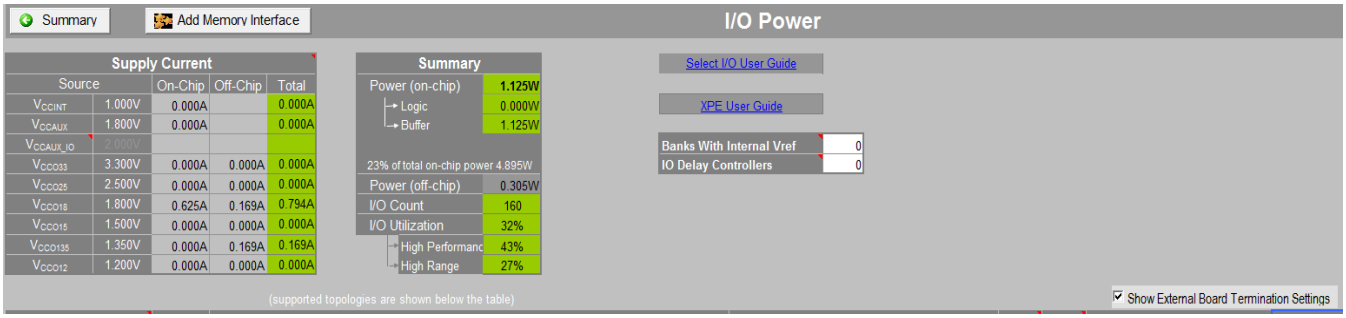


Figure 34: **I/O Sheet - Top Section (7 Series)**

Figure 35 illustrates the three main types of information entered on the I/O sheet: **IO Settings**, **Activity**, and, if needed, **External Termination**.

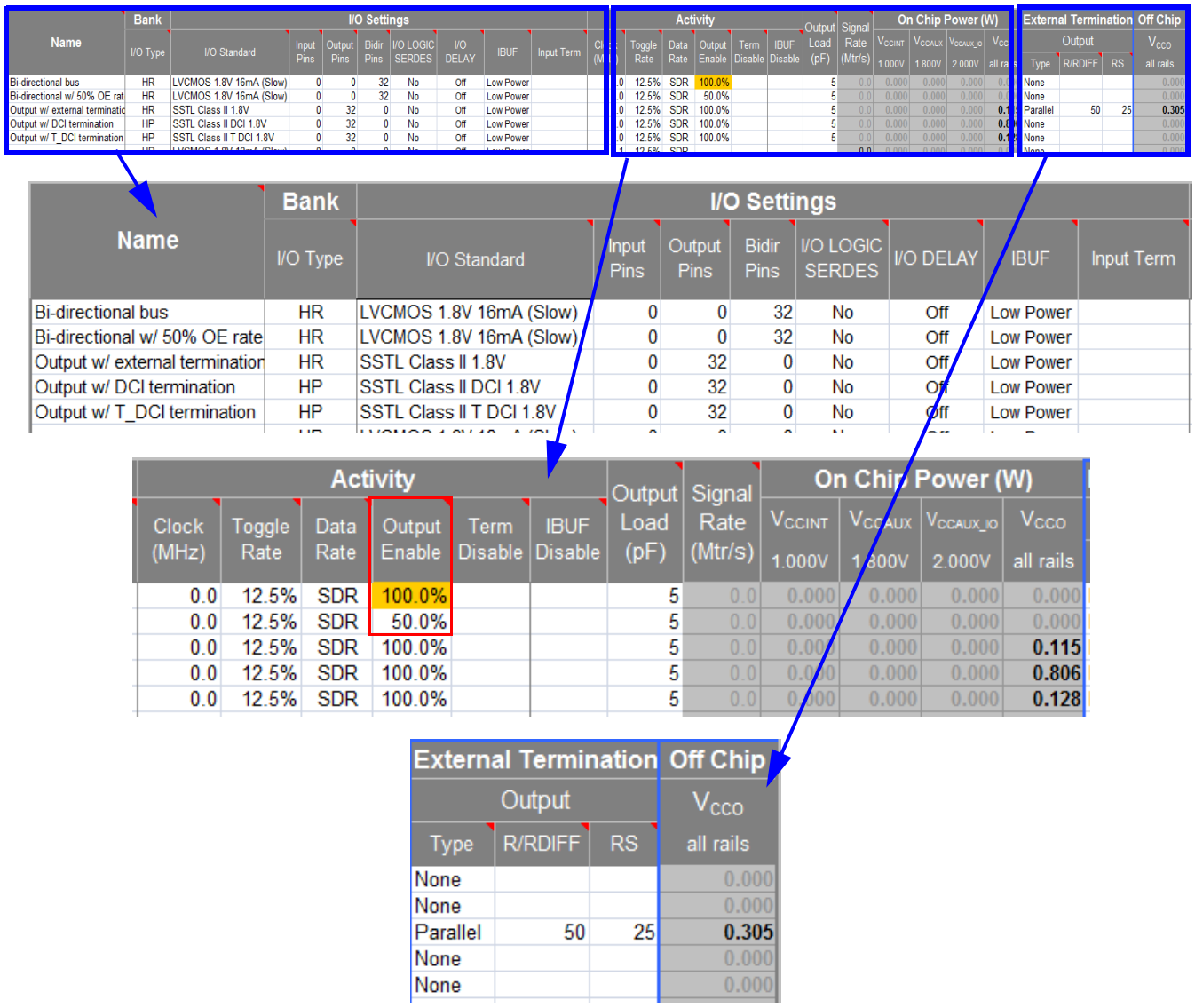


Figure 35: **I/O Sheet - Effect of Output Enable Rate on Power Estimates for Inputs, Outputs, and Bidirectional I/Os (7 Series)**

The following paragraphs provide more information on how to fill in each of these columns.

- **I/O Settings**
  - **I/O Standard**

    Specify here the expected I/O standard you will use for this interface. Configurations which use the on-chip terminations are shown with a **DCI** suffix in this drop-down menu. Differential I/O standards have a **(pair)** suffix. For calculations, XPE assumes the standard V_{CCO} level (for example, 3.3V) that is closest to the nominal listed in the datasheet for that I/O standard.

    Note: For Spartan-6 FPGAs, the open drain standards I2C and SMBUS can use a V_{CCO} from 2.7V to 3.45V, with a 3.0V nominal voltage. In XPE these are calculated using a V_{CCO} of 3.3V.

TIP: *To minimize on output signals always use the weakest driver settings which meet your performance goals (lpowerower the drive strength and slew rate).*

TIP: *Using on-chip terminated standards is a good way to improve the signal integrity of the waveforms seen by the receiver. Since the terminations are embedded inside the FPGA, the termination power will contribute to raising the device junction temperature. In order to minimize this power try to use the tri-statable on-chip terminated standards (denoted **T_DCI**) whenever possible.*

- I/O Direction Columns

  Enter the number of **Input**, **Output** and **Bidir** (bidirectional) signals for each I/O interface.

TIP: *Since toggling activity of inputs and outputs is often very different, Xilinx recommends you place each direction on a separate row.*

TIP: *Enter one pin for each differential I/O pair. For instance, if your memory has four differential DQS pairs, enter **4** on the **Input Pins** column.*

- I/O Performance Settings

  These performance settings, such as **IO LOGIC SERDES** or **IO DELAY**, are family dependent. Enter the configuration in which you expect to program these I/Os.

TIP: *Typically performance settings increase power consumption. Try to enable these setting only if your I/O interface absolutely requires them.*

- **Activity**

  Enter in these four columns the expected activity for each I/O interface.

  - **Clock (MHz)**

    Synchronous signals: Enter the frequency of the clock capturing or generating these signals.

    Asynchronous signals: Calculate the equivalent frequency of the signal. For instance, if you can determine the signal will toggle (change state) 2 million times per second then enter 1 in this column (when converting signal rate to frequency you need 2 transitions to make a period: the transition from 0 to 1 and the transition from 1 to 0).

- **Toggle Rate**

  Synchronous elements: Enter how often compared to the clock this signal is expected to change state. For instance if the data changes every 8 clock cycles on average, enter 12.5% (1/8, converted to a percentage).

  Asynchronous elements: As explained in the **Clock (MHz)** description above, enter the equivalent frequency in the **Clock (MHz)** column then enter 100% in this column.

- **Data Rate**

  Synchronous elements: Enter **DDR** if the signal is sampled on both the positive and negative edges of the clock.

  Asynchronous elements: This column is not applicable (leave value at **SDR**).

- **Output Enable**

  Input only signals: This column has no effect.

  Output and bi-directional signals: Specify for a long period of time how much of this time the output buffer is driving a value (compared to the time the driving buffer is disabled or tri-stated.

TIP: *As shown in Figure 35 (red frame) for line 1 and 2, setting **Output Enable** to **100%** is a common mistake which degrades the tool accuracy.*

- **Signal Rate**

  Defines the number of millions of transitions per second for the considered element. This is a read-only column.

  Signal Rate is computed in this way:

  For Inputs:

  Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Toggle rate (%) * Data Rate

  For Outputs:

  Signal Rate (Mtr/s) = Clock Frequency (MHz) * Toggle Rate (%) * Data Rate * Output Enable Rate (%)

- **External Termination**

  When not using the available on-chip termination you can use XPE to calculate the power supplied by the FPGA to off-chip components such as external board termination resistor networks. When the **Show External Board Termination**

Settings checkbox is checked, additional columns appear in the table. Also, a graphic appears below the table and shows the supported **Output Termination Topologies**, so you can easily understand which column to fill depending on the topology you want to build.

Multiple termination types are supported for I/Os configured as outputs. External input terminations are not supported since calculations often require details of the driver side but these details are not available to XPE.

- **Term. Type**

  Select the appropriate topology from this drop-down menu.

- **R/RDIFF** and **RS**

  Some termination schemes require two resistor values while others require only a single value. Refer to the termination graphic then enter the resistor value on the appropriate column. Figure 36 shows the supported I/O termination topologies in this release.

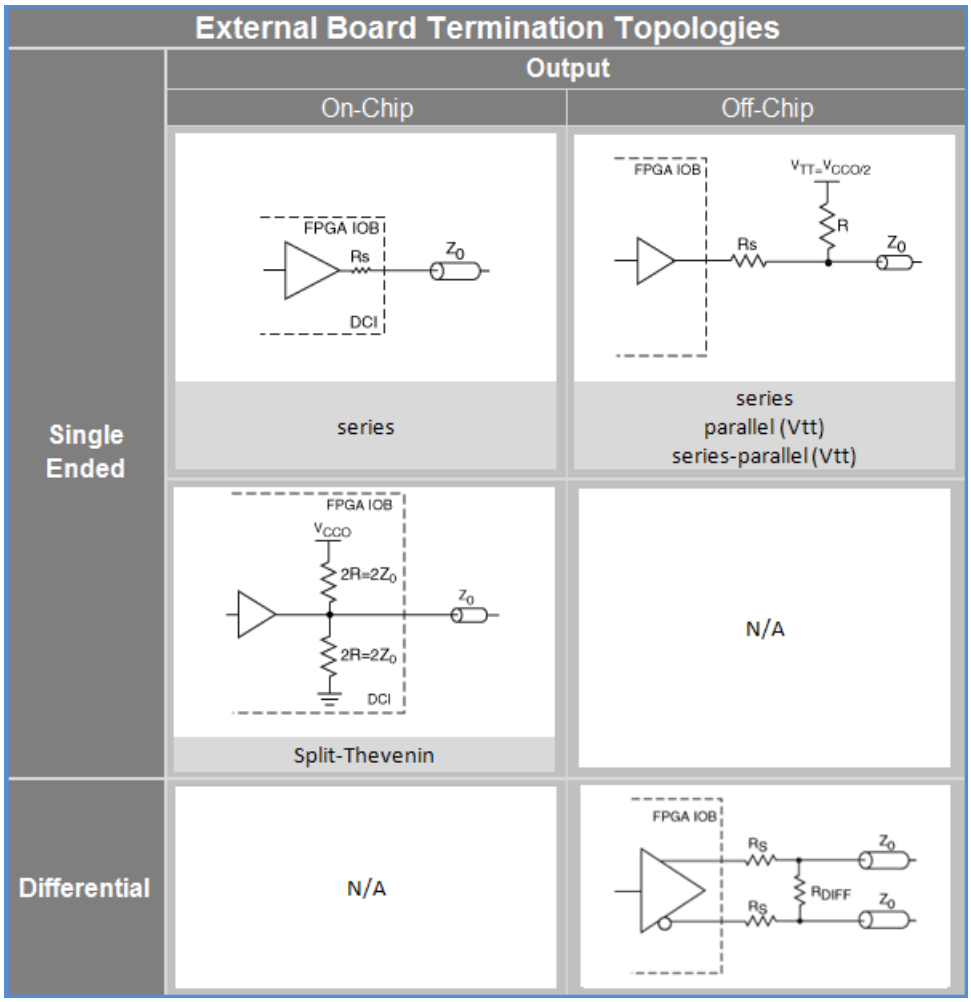


Figure 36: **External I/O Termination Topologies (Virtex-6 and 7 Series)**

Memory Interface Configuration Wizard and the I/O Sheet

For the 7 Series/Zynq-7000 XPE spreadsheet, you can enter information for the I/Os involved in the interface between the FPGA and external memory by using the Memory Interface Configuration wizard. The Memory Interface Configuration wizard provides a simplified method of filling in the memory interface I/Os in the XPE spreadsheet.

When you configure a memory interface using the wizard, rows will be added to the I/O sheet for each output line (for example, Data, Address, and Clock) from the FPGA that will be applied to the external memory.

The Memory Interface Configuration wizard can be started from the I/O sheet by clicking the **Add Memory Interface** button.

For a description of the Memory Interface Configuration wizard and how you can run the wizard from the I/O sheet, see Memory Interface Configuration Wizard, page 34.

To understand the 7 series memory interfaces and the settings you will enter within XPE refer to the *7 Series FPGAs Memory Interface Solutions User Guide (UG586)* [Ref 9].

Block RAM (BRAM) Sheet

FPGA devices have dedicated block RAM resources. To accurately set Block RAM parameters in XPE, a good understanding of device resources and configuration possibilities is recommended. This information is available in the BRAM section of the device family *Device User Guide*. If implementation details for the block RAM are known, follow the guidelines described in Setting BRAM Mode for Improved Accuracy, page 69. Otherwise, refer to Preliminary BRAM Estimates, page 68.

Note: Distributed RAM/ROM and SRL usage should be specified in the Logic Sheet.

To enter information on the Block RAM sheet, you can use the XPE Memory Generator wizard, which appears when you click the **Add Memory** button on the Block RAM sheet. The XPE Memory Generator wizard provides a simplified method of adding rows to the Block RAM sheet. For information about using this wizard, see Memory Generator Wizard and the Block RAM Sheet (Block Memory), page 70.

Some details about columns in the Block RAM sheet:

- **Enable Rate** column

  Use the **Enable Rate** to specify the percentage of time each block RAM's ports are enabled for reading and/or writing. To save power, the RAM enable can be driven Low on clock cycles when the block RAM is not used in the design. BRAM **Enable Rate**, together with **Clock** rate, are important parameters that must be considered for power optimization.

- **Write Rate** column

  The **Write Rate** represents the percentage of time that each block RAM port performs write operations. The read rate is understood to be 100% – write rate.

- **Signal Rate** column

  Defines the number of millions of transitions per second for the considered BRAM output port. This is a read-only column which takes into account port enable rates and a weighted average of the port widths.

Figure 37 illustrates the effect of block RAM configuration modes and bit widths on power estimates.

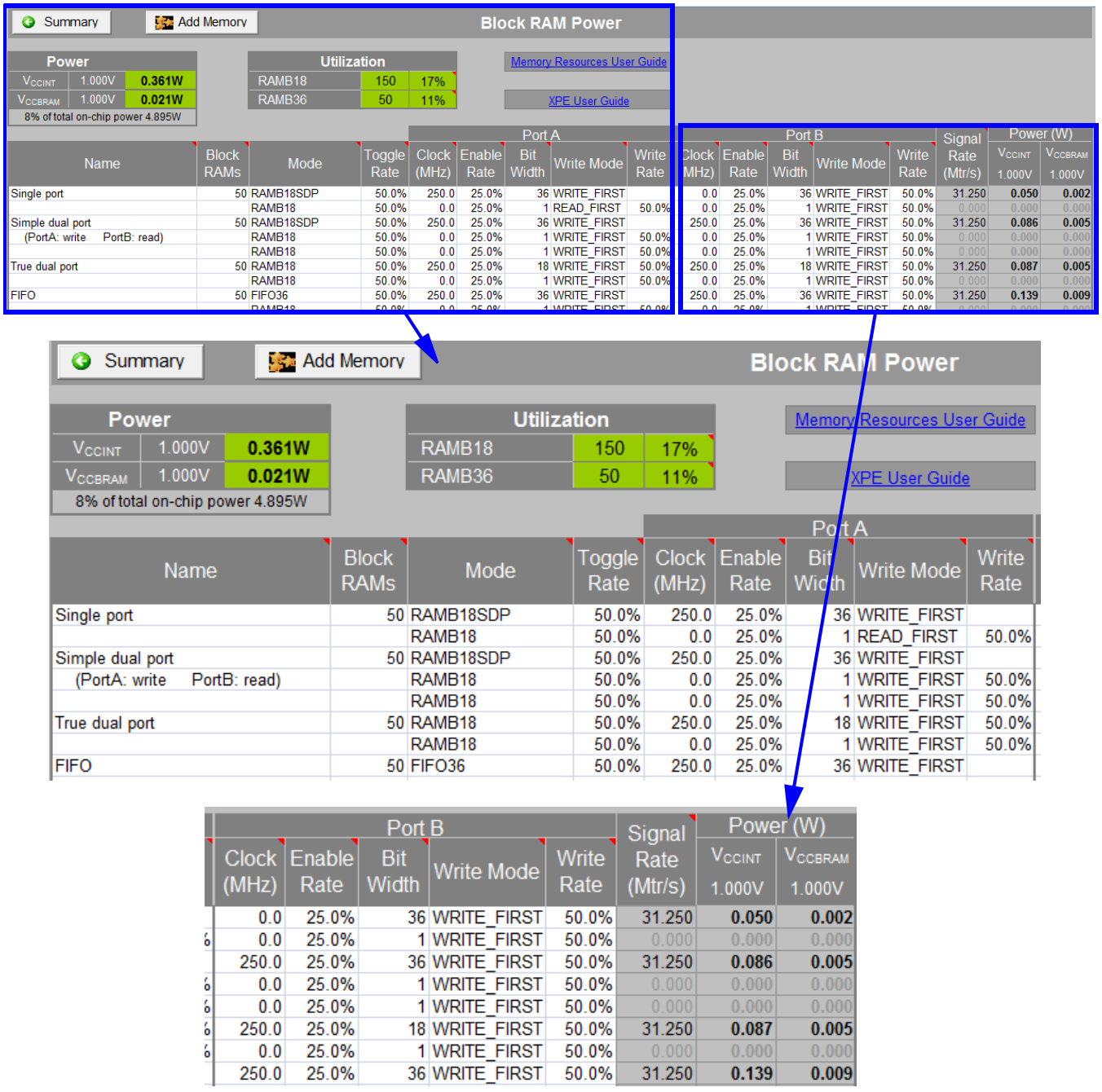


Figure 37: **Block RAM Sheet - Effect of Block RAM Configuration Modes and Bit Widths on Power Estimates (7 Series)**

Preliminary BRAM Estimates

If the exact block RAM types and modes to be used in the design are unknown, the best approach is to determine how many kilobytes of memory are needed in the design and use the appropriate number of basic 18k True dual-port RAMs. If the data width of memory access is known, select this from the drop-down menu for each port. Depth and width are the two most important characteristics of a memory.

Setting BRAM Mode for Improved Accuracy

If the breakdown of the memory usage of your design is known, the XPE spreadsheet allows you to specify which block RAM modes are being used. The **Mode** column has selectable values from a drop-down menu that lists the different ISE primitive names and modes of the block RAM. Depending on the target family, this includes:

- **BRAM** - Simple dual-port or True dual-port Block RAM,
- **FIFO** - Dedicated built-in FIFO,
- **CASC (pair)** - Cascaded block RAM blocks (built from two RAM blocks),
- **ECC** - When the block RAM is configured in ECC mode.

In True dual-port mode the following data write mode options are available:

- **WRITE_FIRST** – The port will first write to the location and then read out the newly written data.
- **READ_FIRST** – The old data is first read out and then the new data is written in. This mode effectively allows 4 operations per clock cycle (saving power or resource utilization), since the old data can be read out and replaced with new data on the same clock cycle of each port. However, note that READ_FIRST is only more power efficient if the data in the memory is used the same time as writing out new data, and does not force separate read and write operations to get the data. If that is not the case, READ_FIRST is generally less efficient in power than NO_CHANGE in TDP mode. If the functionality of READ_FIRST is not needed, the BRAM should be configured as WRITE_FIRST or NO_CHANGE to save power.
- **NO_CHANGE** – When a Write happens the block RAM outputs remain unchanged.

In Simple dual-port mode the following data write mode options are available:

- **WRITE_FIRST** – The port will first write to the location and then read out the newly written data.
- **READ_FIRST** – The old data is first read out and then the new data is written in. This mode effectively allows 2 operations per clock cycle (saving power or resource utilization), since the old data can be read out and replaced with new data on the same clock cycle of each port. However, note that READ_FIRST is only more power efficient if the data in the memory is used the same time as writing out new data, and does not force separate read and write operations to get the data. If that is not the case, READ_FIRST is generally less efficient in power than WRITE_FIRST in SDP mode. If the functionality of READ_FIRST is not needed, the BRAM should be configured as WRITE_FIRST to save power.
- **NO_CHANGE** – Not available in the SDP mode because it is identical in behavior to WRITE_FIRST mode.

Memory Generator Wizard and the Block RAM Sheet (Block Memory)

For the 7 Series/Zynq-7000 XPE spreadsheet, you can enter block memory information in the Block RAM sheet by using the Memory Generator wizard. The Memory Generator wizard provides a simplified method of populating the Block RAM sheet with rows related to block memory, displayed as **BRAMs** on the Block RAM sheet.

The Memory Generator wizard can be started from the Block RAM sheet by clicking the **Add Memory** button.

For a description of the Memory Generator wizard and how you can run the wizard from the Block RAM sheet, see Memory Generator Wizard (for Block Memory), page 31.

To understand the capabilities of the 7 series block memory and the settings you will enter within XPE refer to the *7 Series FPGAs Memory Resources User Guide (UG473)* [Ref 6].

Clock Management Resource Sheets (DCM, PMCD, PLL, MMCM, Clock Manager)

Xilinx FPGA families have different clock generation and management capabilities. To enter information in these sheets, first review the *Device User Guide* to understand how to parameterize these resources in XPE. Depending on the step in the project development cycle you may or may not already know all the clocking details for your design. Enter what is known or can be estimated first, then later you can always reopen and complete the spreadsheet as design details become available.

The clock management resource sheets are presented in a different way in the XPE spreadsheets that support the various FPGA and AP SoC architectures.

- In the 7 Series/Zynq 7000 XPE spreadsheet, information for the two clock managers, MMCM and PLL, is supplied on a single sheet, the Clock Manager Power sheet. An **MMCM or PLL** column in the Clock Manager Power sheet lets you specify whether you are supplying information for the MMCM or the PLL.
- In spreadsheets for earlier devices (for example, the Virtex-5/Virtex-6 spreadsheet or the Spartan-3A/Spartan-6 spreadsheet), there will be a different sheet for each clock manager used. For example, separate DCM Power and PLL Power sheets may be displayed in these earlier spreadsheets.

Figure 38 shows a sample clock management resource sheet (the Clock Manager Power sheet).

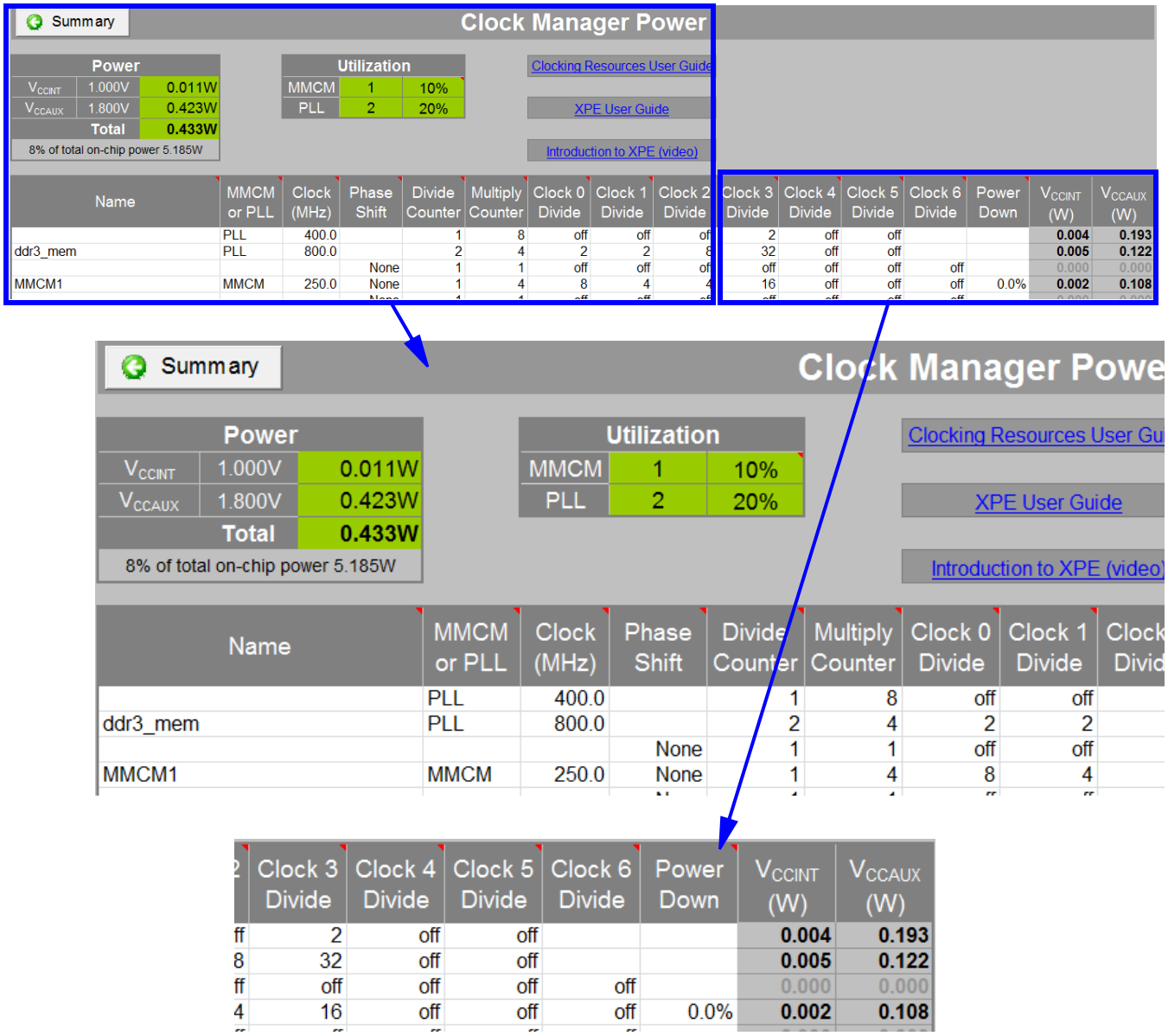


Figure 38: **Clock Manager Power Sheet (7 Series)**

DSP Sheet (MULT, DSP48)

Xilinx FPGA families have different Digital Signal Processing (DSP) blocks with different capabilities. To enter information in these sheets first review the *Device User Guide* to understand the parameters in the DSP sheet.

TIP: *For random input data, a good **Toggle Rate** approximation for DSP operations is 50%.*

TIP: *DSP slices have clock enable (CE) ports. When entering data in the **Toggle Rate** column remember to multiply your data input toggle rate with the DSP slice clock enable rate. For example, if random data (typically ~38% data toggle rate) is input into the DSP slice and the slice is clock enabled only 50% of the time, then the output data toggle rate should be scaled by the CE rate such that the data toggle rate becomes 19% (38% x 50%). see Figure 39 for a Virtex-7 example.*

TIP: *For families which have a register within the multiplier (MREG), using this pipeline register helps lower dynamic power.*

Summary — DSP48Power

Power		
V_{CCINT}	1.000V	0.077W
2% of total on-chip power 4.583W		

Utilization		
DSP48	60	7%

DSP48 User Guide

XPE User Guide

Name	DSP Slices	Clock (MHz)	Toggle Rate	MULT Used?	MREG Used?	Pre-add Used?	Signal Rate (Mtr/s)	Power (W)
Multiplier with pipeline register	20	250.0	12.5%	Yes	Yes	No	31.250	**0.013**
		0.0	12.5%	Yes	Yes	No	0.000	0.000
Multiply accumulate	20	250.0	12.5%	Yes	Yes	Yes	31.250	**0.014**
		0.0	12.5%	Yes	Yes	No	0.000	0.000
DSP with high activity on inputs	20	250.0	50.0%	Yes	Yes	No	125.000	**0.050**
		0.0	12.5%	Yes	Yes	No	0.000	0.000

Figure 39: **DSP48E1 Power Sheet (7 Series) - Effect of Clock, Toggle Rate, and MREG on Power Estimates**

Multi-Gigabit Transceiver Sheets (MGT, GT, GTP, GTX, GTH, GTZ)

Different Xilinx FPGA families have Multi-Gigabit Transceivers (MGT), which are very high performance serial I/Os. Transceivers typically use separate voltage supplies for the PCS, PMA and termination. To understand each family MGT capabilities and how to enter settings within XPE refer to the applicable *Transceiver User Guide*.

IMPORTANT: *In the 7 series/Zynq 7000 XPE spreadsheet, PCI Express (PCIe) information is specified on a GTX, GTP, or GTH sheet. Spreadsheets for earlier Xilinx FPGA devices have a separate PCIe sheet.*

To simplify data entry, drop-down menus are provided with parameter preferred or required values. Figure 40 shows an example Kintex-7 XC7K325T design. The tables in the sheet

header report design power and currents. Device leakage for each supply is reported on the Summary sheet.

For 7 series devices, XPE provides a Transceiver Interface Configuration wizard to allow you to quickly enter the important parameters required for an accurate transceiver power estimate. For step-by-step instructions about how to use the wizard to fill out the MGT sheets, see Transceiver Configuration Wizard, page 38.

XPE calculates power for each channel including the power of all associated circuits, shared resources between channels, IO buffers, reference clock circuitry, etc. You therefore do not have to enter resource usage on any other sheet (for example, Clock or I/O) to describe the transceiver resources used.

XPE presents the MGT information in an architecture-specific way. Entering 2 or any multiple of 2 channels for a GTP/GTX_DUAL entry assumes that those channels use the minimum number of DUALs. Similarly, for GTHE1 and GTXE2 4 channels share common circuitry, so XPE assumes each line uses the minimum number of quads. To use 2 channels from one quad and 2 from another, simply specify them on two rows in XPE.

TIP: *For Spartan-6 FPGAs, you can specify a GTPA1_DUAL with different settings for each channel by entering each channel on a separate row using the same base name suffixed with* ***_0*** *and* ***_1*** *(for example,* ***GTP_0*** *and* ***GTP_1****). A red border around the cells of two adjacent rows indicates the two GTPA1s are inferred to be in the same GTPA1_DUAL.*

The **Power Planes** field in the MGT sheet represents the number of power planes used in the design. MGT transceivers require multiple analog power supplies for the PMA (Physical Medium Attachment). The number of power planes varies by device and package. When not all available MGTs are used, it may be possible to ground unused power planes to reduce the static power.

In the 7 series/Zynq-7000 spreadsheet, the GTX, GTP, and GTH sheets have an **OOB Used** column. The OOB feature uses out-of band (OOB) signaling for PCIe and other protocols where the physical connection may be unplugged during operation. OOB is supported using high-speed amplitude detection on the inputs and squelch on the corresponding outputs. A Yes in the **OOB Used** column indicates that your design will use this feature.

TIP: *For a description of the* ***Eye Scan*** *feature, which you can set to On or Off in the GTX and GTH MGT sheets, see the 7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7].

TIP: *In the 7 Series GTX sheet, you can set the* ***Power Mode*** *for GTX transceivers to Low Power or DFE. For a description of the low-power mode (LPM) and the decision feedback equalization (DFE) mode, see the RX Equalizer (DFE and LPM) section in the 7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7]

XPE does not support all of the possible MGT configurations. See the specific *Transceiver User Guide* for more information.

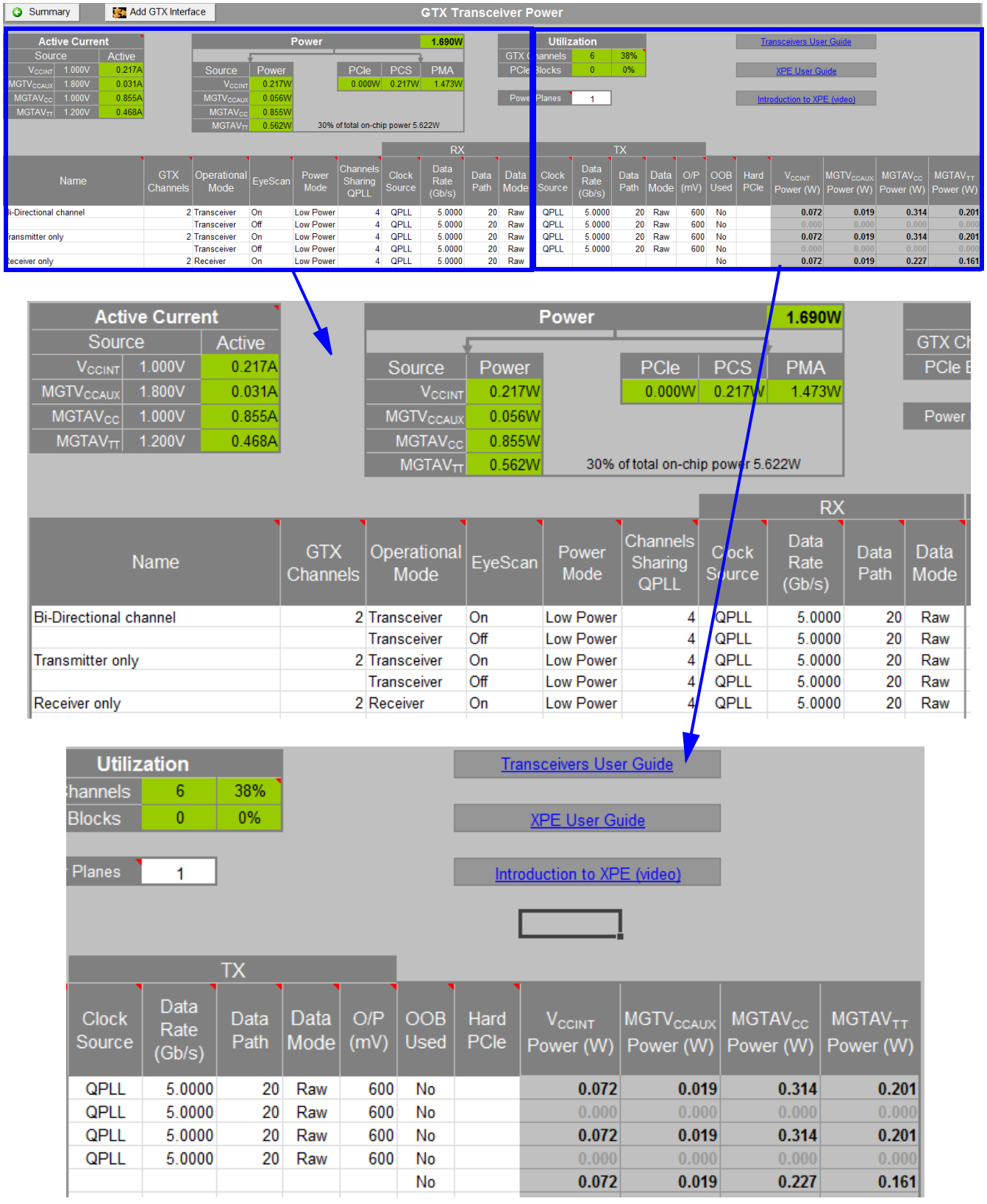


Figure 40: **GT Power Sheet (Kintex-7) Illustrating Data Rate and Power Estimates**

Transceiver Wizard and the MGT Sheet

For the 7 Series/Zynq-7000 XPE spreadsheet, you can enter transceiver information in a GT sheet (GTP, GTH, GTX, or GTZ) by using the Transceiver Configuration wizard. The Transceiver Configuration wizard provides a simplified method of filling in the GT sheets in the XPE spreadsheet.

The Transceiver Configuration wizard can be started from a GT sheet by clicking the **Add GT Interface** button (sample shown below).

For a description of the Memory Generator wizard and how you can run the wizard from the GT sheet, see Transceiver Configuration Wizard, page 38.

To understand the capabilities of the 7 series GTs and the settings you will enter within XPE refer to the *7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)* [Ref 7] and the *7 Series FPGAs GTP Transceivers User Guide (UG482)* [Ref 8].

GT Power Up / Power Down Sequencing

When your design has been programmed into the Xilinx FPGA, the recommended GT transceiver power-on sequence to achieve minimum current draw is specified in the *Data Sheet: DC and Switching Characteristics* for the applicable device. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If the recommended sequences are not followed, current drawn can be higher than specifications during power-up and power-down. XPE calculates GT power assuming the recommended power-up, power-down sequence is used by the design, and the power numbers reflect this.

To calculate the extra power as a result of not following the recommended power up/down sequence, consult the Xilinx *Answer Records*.

TEMAC Sheet

Different Xilinx device families contain Tri-Mode Embedded Ethernet Media Access Controller (MAC) blocks, which are used in Ethernet applications. The Ethernet MACs are paired within a TEMAC block, share a common host and DCR interface, but are independently configurable to meet all common Ethernet system connectivity needs. Refer to the applicable EMAC *User Guide* for a detailed description of the block capabilities and configuration.

In XPE, you need only enter the TEMAC operating clock frequency (See Figure 41). You typically need to know the mode and operating speed to obtain the correct clock frequency.

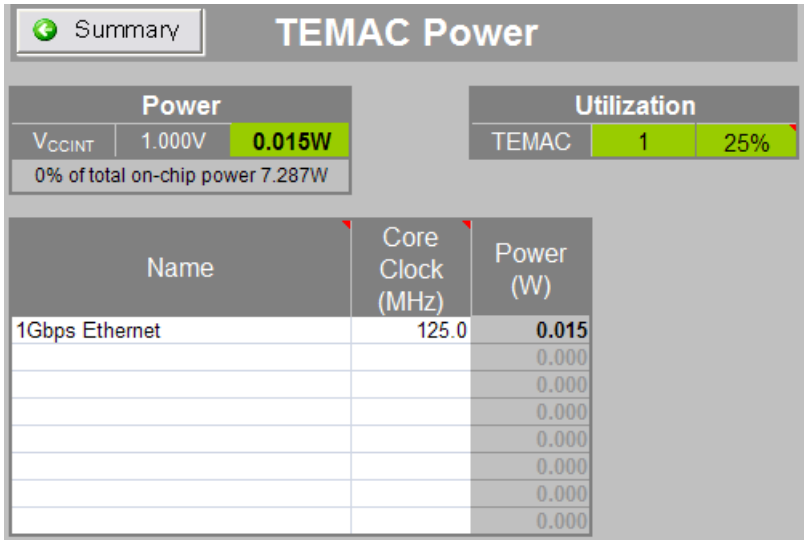


Figure 41: **TEMAC Power Sheet (Virtex-6)**

PCIe Sheet

Different Xilinx device families have Integrated Endpoint Block for PCI Express® designs (integrated Endpoint block). For detailed PCIe information, refer to the applicable PCIe *User Guide* and enter in XPE the settings which correspond to your application.

Note: The 7 series/Zynq 7000 XPE spreadsheet does not have a PCI Express sheet. For these devices, PCIe information is specified on the Multi-Gigabit Transceiver sheets. See Multi-Gigabit Transceiver Sheets (MGT, GT, GTP, GTX, GTH, GTZ).

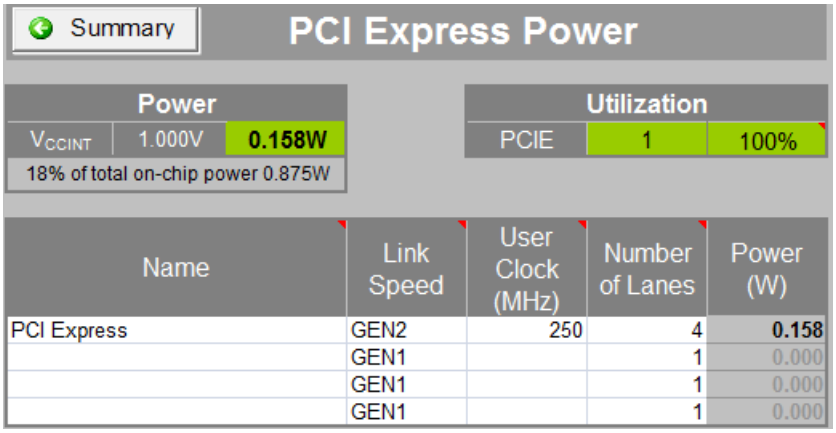


Figure 42: **PCIE Power Sheet (Virtex-6)**

PPC440 (PowerPC) Sheets

Some Xilinx FPGA families contain high-performance PowerPC® microprocessor embedded blocks.

For power estimation, these blocks are represented in a separate sheet within XPE. Details for each PowerPC's settings are available in the applicable *Device User Guide*. Typically you can provide the processor main clock frequency along with details of the processor local bus, memory and eventual DMA controllers. Figure 43 presents a Virtex-5 example.

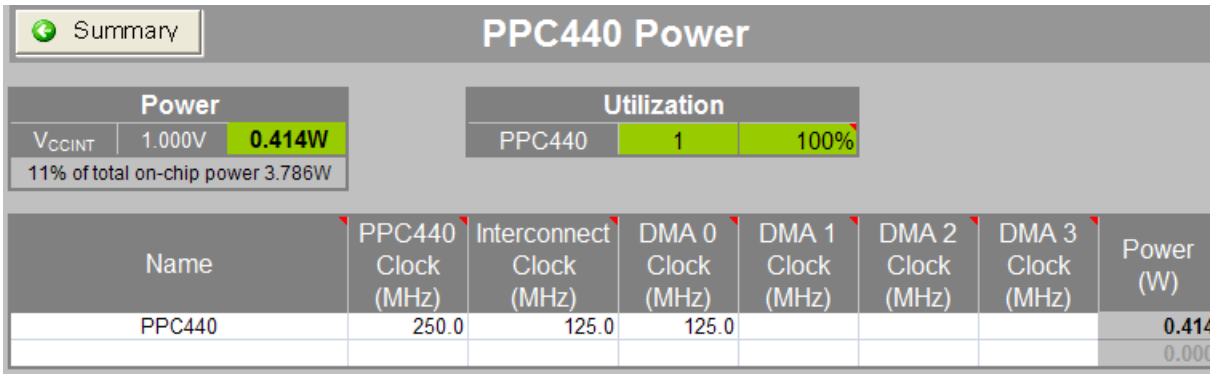


Figure 43: **PPC440 Power Sheet (Virtex-5)**

PS Sheet (Zynq-7000 Only)

The PS sheet allows you to estimate power for the Processor System (PS) in a Zynq-7000 AP SoC device.

The PS has between two and five voltage sources depending on the exact configuration. The V_{CCO_DDR} voltage is dependent on the memory interface selected and the V_{CCO_MIO0} and V_{CCO_MIO1} voltages are dependent on the I/O interfaces and standards used in the respective banks.

The PS in the Zynq-7000 AP SoC is described in the *Zynq-7000 All Programmable SoC Technical Reference Manual (UG585)* [Ref 13].

- **Processor**

  The processor used in the PS is a dual core Cortex A9. The number of **A9 Cores** used and their clock frequency (**Clock (MHz)**) are required information. Processor **Load** of 50% is for average usage and may be adjusted up or down as needed to reflect the processor loading in a specific design.

- **PLLs**

  There are three **PLL**s in the PS that must be set to the correct frequency (**MHz**) when used. By default the **Processor** and **Memory** PLLs run at twice their associated clock frequency.

- **Memory Interface**

  DDR2, DDR3, DDR3L, and LPDDR2 memory interfaces (**Memory Type**) are supported in either 16 or 32 bit **Data Width**. The clock frequency (**Clock (MHz**)) is half the data rate since these are all DDR interfaces. The **Read Rate** and **Write Rate** represent the usage and may be set to any values that together are less than or equal to 100%.

  The **Data Toggle Rate** is the average for the data lines with 50% being random data. The **Output Load** is the board capacitance and the external termination (**External Term**) is the far end parallel termination used for the data lines.

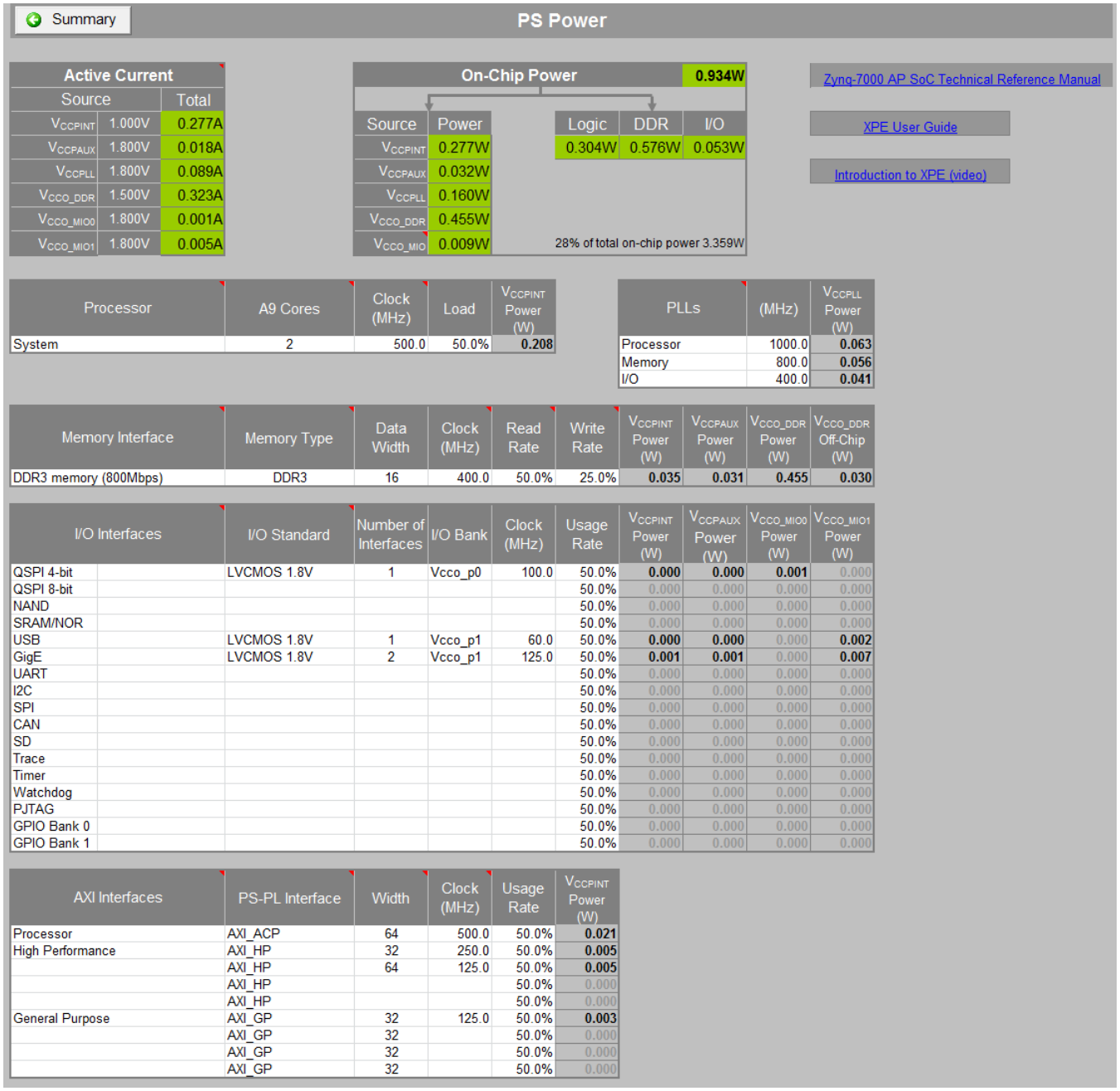
- **I/O Interfaces**

  The PS supports a variety of standard interfaces (**I/O Standard**) and some general purpose I/O. There are two I/O banks and all interfaces on a bank must use the same voltage. Available **I/O Interface**s, **I/O Standard**s, **Number of Interfaces**, and **I/O Bank** placement are represented in the XPE tool.

- **AXI Interfaces**

  The PS side of the AXI interfaces are based on the AXI 3 interface specification. Each interface consists of multiple AXI channels. There are nine AXI interfaces for PS-PL interfacing.

  - AXI_ACP - One cache coherent master port for the PL.
  - AXI_HP - Four high performance/bandwidth master ports for the PL.
  - AXI_GP - Four general purpose ports (two master ports and two slave ports).



Summary

PS Power

Active Current		
Source		Total
V_{CCPINT}	1.000V	0.277A
V_{CCPAUX}	1.800V	0.018A
V_{CCPLL}	1.800V	0.089A
V_{CCO_DDR}	1.500V	0.323A
V_{CCO_MIO0}	1.800V	0.001A
V_{CCO_MIO1}	1.800V	0.005A

On-Chip Power	0.934W			
Source	Power	Logic	DDR	I/O
V_{CCPINT}	0.277W	0.304W	0.576W	0.053W
V_{CCPAUX}	0.032W			
V_{CCPLL}	0.160W			
V_{CCO_DDR}	0.455W			
V_{CCO_MIO}	0.009W			

28% of total on-chip power 3.359W

Zynq-7000 AP SoC Technical Reference Manual

XPE User Guide

Introduction to XPE (video)

Processor	A9 Cores	Clock (MHz)	Load	V_{CCPINT} Power (W)
System	2	500.0	50.0%	**0.208**

PLLs	(MHz)	V_{CCPLL} Power (W)
Processor	1000.0	**0.063**
Memory	800.0	**0.056**
I/O	400.0	**0.041**

Memory Interface	Memory Type	Data Width	Clock (MHz)	Read Rate	Write Rate	V_{CCPINT} Power (W)	V_{CCPAUX} Power (W)	V_{CCO_DDR} Power (W)	V_{CCO_DDR} Off-Chip (W)
DDR3 memory (800Mbps)	DDR3	16	400.0	50.0%	25.0%	**0.035**	**0.031**	**0.455**	**0.030**

I/O Interfaces	I/O Standard	Number of Interfaces	I/O Bank	Clock (MHz)	Usage Rate	V_{CCPINT} Power (W)	V_{CCPAUX} Power (W)	V_{CCO_MIO0} Power (W)	V_{CCO_MIO1} Power (W)
QSPI 4-bit	LVCMOS 1.8V	1	Vcco_p0	100.0	50.0%	**0.000**	**0.000**	**0.001**	0.000
QSPI 8-bit					50.0%	0.000	0.000	0.000	0.000
NAND					50.0%	0.000	0.000	0.000	0.000
SRAM/NOR					50.0%	0.000	0.000	0.000	0.000
USB	LVCMOS 1.8V	1	Vcco_p1	60.0	50.0%	**0.000**	**0.000**	0.000	**0.002**
GigE	LVCMOS 1.8V	2	Vcco_p1	125.0	50.0%	**0.001**	**0.001**	0.000	**0.007**
UART					50.0%	0.000	0.000	0.000	0.000
I2C					50.0%	0.000	0.000	0.000	0.000
SPI					50.0%	0.000	0.000	0.000	0.000
CAN					50.0%	0.000	0.000	0.000	0.000
SD					50.0%	0.000	0.000	0.000	0.000
Trace					50.0%	0.000	0.000	0.000	0.000
Timer					50.0%	0.000	0.000	0.000	0.000
Watchdog					50.0%	0.000	0.000	0.000	0.000
PJTAG					50.0%	0.000	0.000	0.000	0.000
GPIO Bank 0					50.0%	0.000	0.000	0.000	0.000
GPIO Bank 1					50.0%	0.000	0.000	0.000	0.000

AXI Interfaces	PS-PL Interface	Width	Clock (MHz)	Usage Rate	V_{CCPINT} Power (W)
Processor	AXI_ACP	64	500.0	50.0%	**0.021**
High Performance	AXI_HP	32	250.0	50.0%	**0.005**
	AXI_HP	64	125.0	50.0%	**0.005**
	AXI_HP			50.0%	0.000
	AXI_HP			50.0%	0.000
General Purpose	AXI_GP	32	125.0	50.0%	**0.003**
	AXI_GP	32		50.0%	0.000
	AXI_GP	32		50.0%	0.000
	AXI_GP	32		50.0%	0.000

Figure 44: **PS Power Sheet (Zynq-7000)**

Other Sheet (7 Series and Zynq-7000)

The Other sheet allows you to calculate the power associated with these device features:

- **XADC** - The XADC (Xilinx® Analog-to-Digital Converter) is the basic building block that enables agile mixed signal functionality in Xilinx® 7 series devices. The XADC includes a dual 12-bit, 1 Mega sample per second (MSPS) ADC and on-chip sensors.

  In the 7 series or Zynq-7000 device, the XADC can be powered down if unused, to save power. In the **XADC** table, set **Powered Down** to Yes if the XADC will be powered down by setting the power down bits in the device's configuration register or by disconnecting the V_{CCADC} supply. Set **Powered Down** to No if the XADC will not be powered down.

  XADC Clock (MHz) specifies the frequency of the DRP clock if your design uses the XADC. Leave this blank if your design does not instantiate the XADC or the XADC is powered down.

  The XADC is described in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide (UG480)* [Ref 16].

- **Config** - The **Config** (Configuration) table allows you to specify these device configuration features:

  - **Readback CRC Clock (MHz)** - Xilinx 7 series devices include a feature to do continuous readback of configuration data in the background of a user design. This feature is aimed at simplifying detection of Single Event Upsets (SEUs) that cause a configuration memory bit to flip and can be used in conjunction with the FRAME ECC feature for advanced operations such as SEU corrections. In the **Config** table, enter the **ReadBack CRC Clock** frequency to include this feature in the XPE power estimate. Leave this blank if your design does not use the Readback CRC feature.

    Readback CRC is described in the *7 Series FPGAs Configuration User Guide (UG470)* [Ref 17].

  - **Config Bank Voltage** - Specifies the setting of the Configuration Bank Voltage Select (CFGBVS), which determines the I/O voltage operating range and voltage tolerance for the configuration-related I/O banks in the device.

    Configuration bank voltage is described in the *7 Series FPGAs Configuration User Guide (UG470)* [Ref 17].

- **PHASER** - Phaser blocks are available in 7 Series devices to simplify the interface with high-speed memory devices. For power estimation, these blocks are represented in a table on the Other sheet. Details for each Phaser setting are available in the *7 Series FPGAs Memory Interface Solutions User Guide (UG586)* [Ref 9].

  In the Phaser table, the **Phaser INs** column is used to specify the number of PHASER_IN and PHASER_IN_PHY blocks used. Similarly, the **Phaser OUTs** column is used for both PHASER_OUT and PHASER_OUT_PHY blocks.

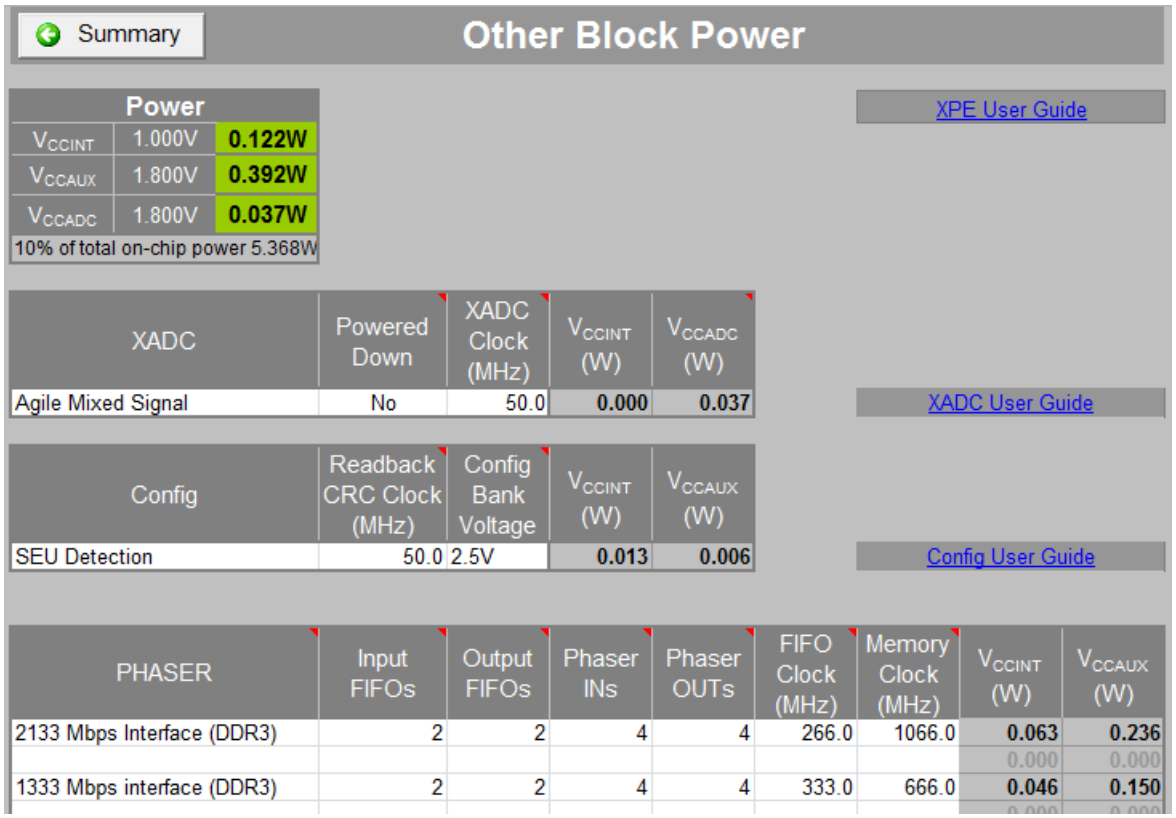


Figure 45: **Other Power Sheet (7 Series)**

User Sheet

This sheet is intentionally left blank and user editable. On this sheet you can provide any documentation (text, image or hyperlinks), details about the project, assumed conditions, or collect the results important to your application.

Automating XPE

To simplify data entry and export or to assist with data manipulation Microsoft Excel offers a variety of mechanisms which you can use to increase your productivity or the breadth of your power estimation and analysis. The following section provides reference material and examples to help you get started quickly with Excel internal automation features and interface with some of the most common external scripting languages.

Using Named Cells

Excel provides a mechanism to name a cell or a range of cells so these can be used within formulae or scripts without referring to them as cell XY coordinates. Since the XPE spreadsheet is protected you cannot see 'named' cells defined on the protected areas. You can however name cells in the unprotected area (User sheet). The following tables and examples show the named cells within XPE that are available to facilitate user formulas and scripting.

Get available resource counts.

The following named cells represent the maximum available resources available for the considered device and package. None of these cells are visible in the spreadsheet, however you can use these read only values in your calculations.

Resource	Named Cells	Description
LUTs	NUM_LUTS	Includes all LUTS
	NUM_LUTRAM	Shift Registers and Distributed Memories LUTs
Registers	NUM_FFS	
DSP blocks	NUM_DSPS	
BlockRAMs	NUM_BRAMS	
PLLs	NUM_PLLS	
MMCMs	NUM_MMCMS	
DCMs	NUM_DCMS	
Transceivers	NUM_GTPS	Lowest speed blocks
	NUM_GTS	Lower speed blocks
	NUM_GTHS	High Speed blocks
	NUM_GTZS	Highest Speed blocks

Examples:

Formulas to quickly set device utilization and evaluate thermal effects when varying device, package or cooling parameters:

= INT(NUM_LUTS * 0.75)	Sets total LUT utilization to 75% of device capacity (if entered on the Logic sheet)
= INT(NUM_DSPS * 0.90)	Sets DSP block utilization to 90% of device capacity (if entered in DSP sheet)

Get device operating limits.

The following named cells represent operating limits for the considered device, package, speed grade and temperature grade. None of these cells are visible in the spreadsheet however you can use these read only values in your calculations.

Table 4: **Operating Limits - Named Cells**

Resource	Named Cells	Description
Temperature	TJ_MAX	Maximum operating junction temperature (°C)
	TJ_MIN	Minimum operating junction temperature (°C)
Voltages	VCC_MAX	Maximum operating V_{CCINT} voltage (V)
	VCC_MIN	Minimum operating V_{CCINT} voltage (V)
Transceivers	GTP_MAXRATE	Maximum data rate of lowest speed blocks (Gbps)
	GTX_MAXRATE	Maximum data rate of lower speed blocks (Gbps)
	GTH_MAXRATE	Maximum data rate of high speed blocks (Gbps)
	GTZ_MAXRATE	Maximum data rate of highest speed blocks (Gbps)

Example:

Formula to enter into the user **Junction Temperature** cell on the Summary sheet to force the device junction temperature to the maximum allowed while evaluating different temperature or device and package combination:

```
= TJ_MAX
```

Get and edit summary information.

Many cells in the Summary sheet or tables at the top of the other sheets are named. To find these names in Excel you can select the cell then if it is named the 'name box' area of the formula bar will show that name. The following paragraph highlights some of the most commonly used cells on the Summary sheet.

Table 5: **Summary Panel - Named Cells (See Figure 24)**

Named Cell	Description
JUNCTION_TEMP	Estimated or forced **Junction Temperature** (°C)
THERMAL_MARGIN_C	Temperature margin for the device temperature grade (°C)
TJA	Estimated or specified **Effective ΘJA** (°C/W)
TOTAL_POWER	**Total On-Chip Power** (W)
THERMAL_MARGIN_W	Power margin for the device temperature grade (W)
OFFCHIP_POWER	Total power supplied to off-chip devices (W)

Table 6: **On-Chip Power Panel - Named Cells (See Figure 23)**

Named Cell	Description
CLOCK_POWER	Clock tree power (W)
LOGIC_POWER	CLB Logic power (W)
BRAM_POWER	BlockRAM power
DSP_POWER	DSP blocks power (W)
PLL_POWER	PLL blocks power (W)
MMCM_POWER	MMCM blocks power (W)
PHASER_POWER	PHASER blocks power (W)
PCIE_POWER	PCIE blocks power (W)
IO_POWER	SelectIO blocks power (W)
GTP_POWER	Lowest speed transceiver blocks power (W)
GTX_POWER	Lower speed transceiver blocks power (W)
GTH_POWER	High speed transceiver blocks power (W)
GTZ_POWER	Highest speed transceiver blocks power (W)
STATIC_POWER	Device static power (W)
PS_POWER	Zynq-7000 processing system (PS) power (W)
PS_STATIC	Zynq-7000 PS device static power (W)
PL_STATIC	Zynq-7000 programmable logic (PL) device static power (W)

Table 7: **Power Supply Panel - Named Cells (See Figure 23)**

Named Cell	Description
VCCINT	V_{CCINT} core voltage level (V)
VCCBRAM	V_{CCBRAM} voltage level (V)
VCCAUX	V_{CCAUX} voltage level (V)
VCCAUX_IO	V_{CCAUX_IO} voltage level (V)
VCCO33	V_{CCO} 3.3V voltage level (V)

Table 7: **Power Supply Panel - Named Cells (See Figure 23)**

Named Cell	Description
VCCO25	V_{CCO} 2.5V voltage level (V)
VCCO18	V_{CCO} 1.8V voltage level (V)
VCCO15	V_{CCO} 1.5V voltage level (V)
VCCO135	V_{CCO} 1.35V voltage level (V)
VCCO12	V_{CCO} 1.2V voltage level (V)

Table 8: **Environment Table - Named Cells (See Figure 22)**

Named Cell	Description
AMBIENT_TEMP	Ambient temperature (°C)
BOARD_TEMP	Board temperature (°C)
CUSTOMTSA	User specified Theta SA thermal resistance (°C/W)
CUSTOMTJB	User specified Theta JB thermal resistance (°C/W)

Table 9: **Miscellaneous Named Cells**

Named Cell	Description
PROJECT	User description of the spreadsheet
VERSION	Spreadsheet revision
RELEASE_DATE	Spreadsheet release date

Using Formulas

With Excel formulas you can simplify data entry, spreadsheet parameterization or create customer reports as explained in the following examples

Example1: Set clock frequency of all attached synchronous loads in a single place.

Typically a clock net may reach multiple types of resources. Instead of entering the clock frequency on each sheet the following formula can be used on the resource sheets while the clock frequency is only defined once in the Clock sheet. Any change of the clock frequency would immediately be reflected on all the linked resource sheets

```
=CLOCK!E19
```

Example 2: Calculate the fanout sum of all the different loads driven by a clock.

On the clock sheet you may find it useful to enter formulas similar to:

```
=SUM(LOGIC!G10:I10,BRAM!E10,DSP!E8)
=SUM(IO!I10:K12)
```

Example 3: Select the GTX data rates to the PCIe interface speed and number of lanes. Entering the following formulae for GTX line rate and number of channels will track the PCIe interface.

- Set channel data rate based on the PCIE bock configuration (if entered on the GTX sheet)

```
=IF(PCIE!E8="GEN3",8,IF(PCIE!E8="GEN2",5,2.5))
```

- Set the number of GTX channels to reflect the number of PCIE lanes (if entered on the GTX sheet)

```
=PCIE!G8
```

Example 4: Parameterize the spreadsheet entry using formulas and the **User** sheet. Figure 46 illustrates how to evaluate power when a module is replicated more or fewer times in the design. By varying the number of instances, the quantity of resources for the base blocks, or clock frequency, an Excel formula can automatically recalculate the values which need to be entered in other sheets. In Figure 46, the value for **Number instance** (named **num_inst**) in the **User** sheet automatically calculates utilization and activity for cells that appear in the **Logic** sheet.

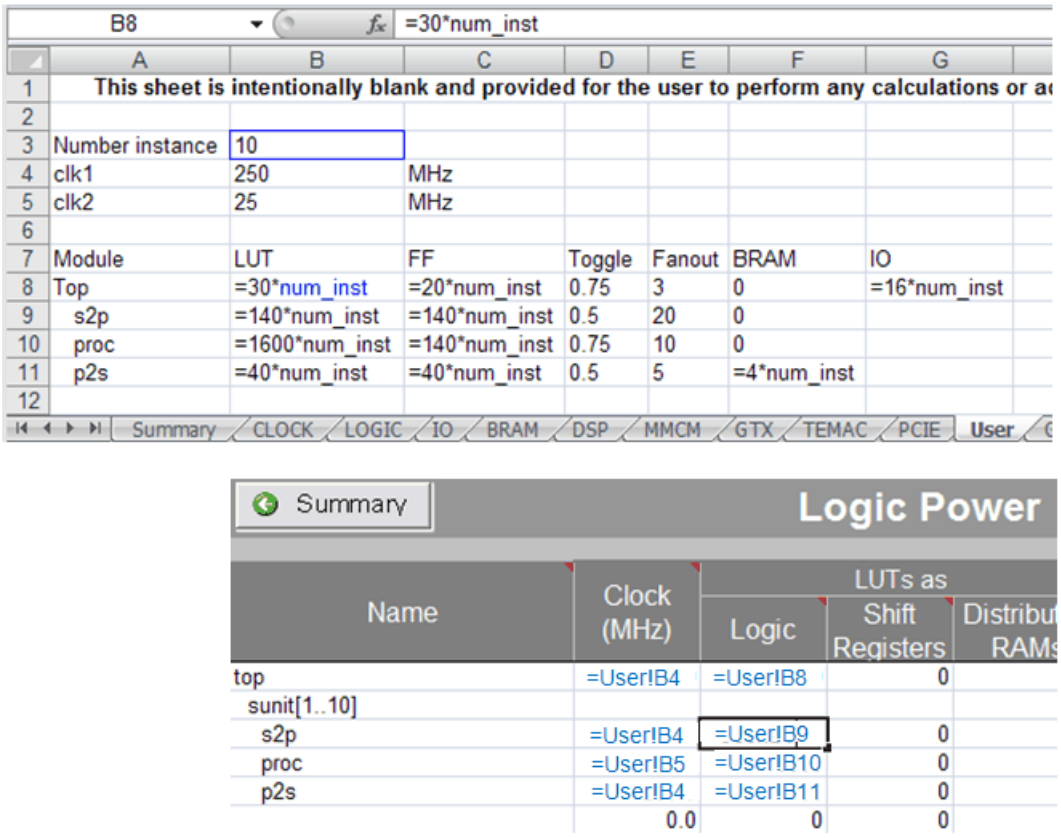


Figure 46: **Parameterizing Data Entry Using Formulas on the User Sheet**

Using Visual Basic Macros

The following examples define the public Visual Basic functions defined in the Xilinx 7 series XPE spreadsheet to help you with your automation needs. They provide convenient ways to load files, create power reports, change parts, packages and environment settings from Excel or another program.

- Create a text power report and save with name specified as argument.

```
Public Sub GeneratePowerReportFile(FileName As String)
```

- Create a settings file and save with name specified as argument. This file can later be used in XPower Analyzer.

```
Public Sub GenerateXPAFile(FileName As String)
```

- Create an XPE file and save with name specified as argument. This file can later be used to restore the current settings in XPE.

```
Public Sub GenerateXPEFile(FileName As String)
```

- Import an existing XPE spreadsheet (.xls* path/file specified as argument).

```
Public Sub ImportXPEFile(path As String)
```

- Import a place and route map report (.mrp path/file specified as argument).

```
Public Sub ImportMapReportFile(FileName As String)
```

- Import a implementation results in the .xpe format. Review the Import dialog options for details and format of the different arguments.

```
Public Sub ImportXmlFile(FileName As String, Append As Boolean,DevSettings As
Boolean, EnvSettings As Boolean, VoltSettings As Boolean, IOSettings As Boolean)
```

- Set the default voltages for all supply voltages. Set argument to False for Nominal voltages and to true for Maximum voltage levels.

```
Public Sub SetDefaultVoltages(Maximum As Boolean)
```

- Set the **Device** field on the Summary sheet (will automatically adjust the **Family** field if required).

```
Public Function SetDevice(Device As String) As Boolean
```

- Set the **Package** field on the Summary sheet.

```
Public Function SetPackage(Package As String) As Boolean
```

- Set the **Process** field on the Summary sheet. Set argument to False for Typical process and True for Maximum process.

```
Public Sub SetProcess (Maximum As Boolean)
```

- Set the **Temp Grade** field on the Summary sheet. Options are "Commercial", "Industrial", "Q-Grade", "Extended", etc.

```
Public Function SetTemperatureGrade (Grade as String) as Boolean
```

- Set the **Speed Grade** field on the Summary sheet. Options are "-1", "-1L", etc.

```
Public Function SetSpeedGrade (Grade as String) as Boolean
```

- Set the **Heat Sink** field on the Summary sheet. Options are "Custom", "None", "Low Profile"

```
Public Function SetHeatSink (Sink as String) as Boolean
```

- Set the **Board Selection** field on the Summary sheet. Options are "Custom", "JEDEC", "Small", "Medium", "Large".

```
Public Function SetBoard (BoardSize as String, BoardLayers as Integer) as Boolean
```

- Set the **User Override** for the **Junction Temperature**, and value.

```
Public Function SetJunctionTemperature(Temperature As Double, OverRide As
Boolean) As Boolean
```

- Set the **User Override** for the **Effective ThetaJA**, and value.

```
Public Function SetEffectiveThetaJA(ThetaJA As Double, OverRide As Boolean) As
Boolean
```

Scripting XPE

Microsoft Excel capabilities described in the previous paragraphs can be accessed from any framework with access to the COM interface. This Component Object Model (COM) is a binary interface standard for software that enable interprocess communications in a large range of programming languages (for example, Visual Basic, Perl, Java). The following examples illustrate how you can set XPE environment parameters, run calculations and read or export results from different languages.

Visual Basic Scripting Example

This simple example opens XPE, then export results into a text power report using the Visual Basic scripting language.

```
Dim XPE As Workbook
XPEfilename = "C:\\Power\\7_Series_XPE_13_1.xls"

On Error Resume Next
Set XPE = Workbooks(XPEfilename)
   ' Opening XPE
   On Error GoTo 0
   If (XPE Is Nothing) Then
      Set XPE = Application.Workbooks.Open(XPEfilename, UpdateLinks:=vbFalse,
ReadOnly:=vbTrue)
      If XPE Is Nothing Then ' Open failed
```

```
            MsgBox ("XPE Open Failed: " & XPEfilename & "Err=" & Err)
            Exit Function
        End If
    End If
' Set Vccint voltage
XPE.Sheets("Summary").Range("VCCINT").Value = myVccint
TotalPower = XPE.Sheets("Summary").Range("TOTAL_POWER").Value
' Export XPE results into a text power report
XPESub = "'" & XPE.Name & "'!" & "ThisWorkBook.GeneratePowerReportFile"
Application.Run(XPESub, FileName)
```

Perl Scripting Example

This simple example opens XPE then export results into a text power report using Perl scripting language.

```
use Win32::OLE;
use Win32::OLE::Const 'Microsoft Excel';

my $myXPEfilename = "C:\\Power\\7_Series_XPE_13_1.xls";

# Opening XPE
my $Excel = Win32::OLE->GetActiveObject('Excel.Application')
    || Win32::OLE->new('Excel.Application', 'Quit');
my $Book = $Excel->Workbooks->Open($myXPEfilename);
# Export XPE results into a text power report
$Excel->Run("ThisWorkBook.GeneratePowerReportFile", "$path/${design}.pwr");
```

Conclusion

The ability to estimate power consumption in a design is imperative for efficient part selection, board design, and system reliability.

The Xilinx Power Estimator tool with its up to date power models and ease of use features is meant to guide and simplify design utilization entry. Although gathering FPGA utilization data may seem difficult in the early design development phases, with a little thought and using XPE, accurate power estimations can be derived. XPE simplifies device selection and helps parallel development of the FPGA logic and the Printed Circuit Board. Finally, XPE helps exploration of alternative implementation and resource configuration when supply power or thermal budgets are exceeded.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

1. *XPower Analyzer Help*
2. *Vivado Design Tools User Guide: Power Analysis and Optimization* (UG907)
3. *Power Methodology Guide* (UG786) - For ISE Design Tools
4. *Command Line Tools User Guide* (UG628) - For ISE Design Tools
5. *7 Series FPGAs Configurable Logic Block User Guide* (UG474)
6. *7 Series FPGAs Memory Resources User Guide* (UG473)
7. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
8. *7 Series FPGAs GTP Transceivers User Guide* (UG482)
9. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)

10. *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS183)
11. *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS182)
12. *Artix-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS181)
13. *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)
14. *Device Package User Guide* (UG112)
15. 7 *Series FPGAs SelectIO Resources User Guide* (UG471)
16. *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480)
17. *7 Series FPGAs Configuration User Guide* (UG470)
18. Descriptions of the resources available in an FPGA can be found under **Silicon Devices** at http://www.xilinx.com/documentation.
19. *Vivado Design Suite Video Tutorials* (http://www.xilinx.com/training/vivado/index.htm)
20. *Vivado Design Suite Documentation* (www.xilinx.com/support/documentation/dt_vivado_vivado2013-3.htm)