

# **ISE Design Suite 14: Release Notes, Installation, and Licensing**

**UG631 (v14.7) October 2, 2013**



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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/02/2013	14.7	Device, tool, and software updates.
06/19/2013	14.6	Device, tool, and software updates.
03/20/2013	14.5	Device, tool, and software updates. Architectures, compatible third-party tools, and system requirements updates. Installation, WebTalk, and licensing content added.

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# Release Notes 14.7

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## What's New

ISE® Design Suite is a proven and mature development environment for All Programmable devices. With the 14.7 release, it now moves into the sustaining phase of its product life cycle. In the future, while there are no more planned ISE major releases, you will continue to receive Xilinx's superior technical support and Xilinx may release periodic updates and patches. If you have not already done so, Xilinx recommends signing up for "My Alerts" at <http://www.xilinx.com/support/answers/18683.htm> to keep you informed.

For new design starts with 7 series and Zynq®, Xilinx recommends that customers migrate to the Vivado® Design Suite. This will allow customers to take advantage of the improved productivity and quality of results found in the new UltraFAST design methodology for Vivado. For new designs on pre 7 series devices, ISE licenses will continue to be provided when purchasing Vivado Design Suite.

## Limited Access Devices

The following devices are Limited Access that require a special license:

- Zynq®-7000
  - 7Z100
- Virtex®-7
  - VX1140T, 2000T, H580T and H870T



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**IMPORTANT:** *The device Zynq-7000 7Z030 in the SBG485 package is often used as a migration for the Zynq-7000 7Z015 devices. The Zynq-7000 7z015 devices are not supported in ISE Design Suite and you should use Vivado Design Suite to target this device*

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# Important Information

## Limited Access Devices

The following devices are fully supported in Vivado, but are limited access in ISE. A special license is required for their use in ISE.

- Zynq-7000
  - 7Z100
- Virtex®-7
  - VX1140T, 2000T, H580T and H870T

## Vivado IP Catalog

Readme files included with IP provided through the Vivado IP Catalog and ISE CORE Generator™ tools have been updated to show a running history of new feature additions.

## Updates to Existing IP

- AXI-PCIe IP moved to production
- 1000BASE-X/SGMII
  - Virtex-7, Artix-7 and Zynq-7000 moved to production
- GMII to RGMII
  - Zynq-7000 moved to production
- QSGMII
  - Virtex-7 Kintex-7, Artix-7 and Zynq-7000 moved to production
- 10G Ethernet MAC
  - Artix-7 moved to production
- XAUI
  - Artix-7 and Zynq-7000 moved to production
- RXAUI
  - Artix-7 and Zynq-7000 moved to production
- 10G Ethernet PCS/PMA (10GBASE-R)
  - Virtex-7, Kintex-7 and Zynq-7000 moved to production
  - 10GBASE-KR access in Vivado only

# Architecture Support and Requirements

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## Operating Systems

Xilinx only supports the following operating systems on x86 and x86-64 processor architectures.

### Microsoft Windows Support

- Windows XP Professional (32-bit and 64-bit), English/Japanese
- Windows 7 Professional (32-bit and 64-bit), English/Japanese
- Windows Server 2008 (64-bit)

### Linux Support

- Red Hat Enterprise Workstation 5 (32-bit and 64-bit)
- Red Hat Enterprise Workstation 6 (32-bit and 64-bit)
- SUSE Linux Enterprise 11 (32-bit and 64-bit)

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## Architectures

The following table lists architecture support for commercial products in the ISE® Design Suite WebPACK™ tool versus all other ISE® Design Suite editions. For non-commercial support:

- All Xilinx® Automotive devices are supported in the ISE Design Suite WebPACK tool.
- Xilinx Defense-Grade FPGA devices are supported where their equivalent commercial part sizes are supported.

Table 2-1: Architecture Support

	ISE WebPACK Tool	ISE Design Suite (All Other Editions)
Zynq® Device	Zynq-7000 Device • XC7Z010, XC7Z020, XC7Z030	Zynq-7000 Device • All
Virtex® FPGA	Virtex-4 FPGA • LX: XC4VLX15, XC4VLX25 • SX: XC4VSX25 • FX: XC4VFX12  Virtex-5 FPGA • LX: XC5VLX30, XC5VLX50 • LXT: XC5VLX20T - XC5VLX50T • SXT: None • FXT: XC5VFX30T  Virtex-6 FPGA • LXT: XC6VLX75T  Virtex-7 FPGA • None	Virtex-4 FPGA • All  Virtex-5 FPGA • All  Virtex-6 FPGA • All  Virtex-7 FPGA • All non-SSIT devices
Kintex™ FPGA	Kintex-7 FPGA • XC7K70T, XC7K160T	Kintex-7 FPGA • All
Artix™ FPGA	Artix-7 FPGA • XC7A100T, XC7A200T	Artix-7 FPGA • All
Spartan® FPGA	Spartan-3 FPGA • XC3S50 - XC3S1500(L)  Spartan-3A/-3AN/-3E FPGA • All  Spartan-3A DSP FPGA • XC3SD1800A  Spartan-6 FPGA • XC6SLX4 - XC6SLX75T	Spartan-3 FPGA • All  Spartan-3A/-3AN/-3E FPGA • All  Spartan-3A DSP FPGA • All  Spartan-6 FPGA • All
CoolRunner™ XPLA3, CoolRunner-II, XC9500 CPLD	• All	• All



# Compatible Third-Party Tools

Table 2-2: Compatible Third-Party Tools

Third-Party Tool	Red Hat Linux	Red Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP 64-bit	Windows-7 32-bit	Windows-7 64-bit
<b>Simulation</b>							
Mentor Graphics ModelSim PE/DE/SE (10.2a)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mentor Graphics ModelSim PE (10.1b)	N/A	N/A	N/A	Yes	Yes	Yes	Yes
Mentor Graphics Questa Advanced Simulator(10.1b)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Cadence Incisive Enterprise Simulator (IES) (12.20.016)	Yes	Yes	Yes	N/A	N/A	N/A	N/A
Synopsys VCS and VCS MX 2(013.06-3*) *- Contact Synopsys for availability of Synopsys VCS	Yes	Yes	Yes	N/A	N/A	N/A	N/A
The MathWorks MATLAB® and Simulink® with Fixed-Point Toolbox (2012a, 2012)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Aldec Active-HDL (9.2)	N/A	N/A	N/A	Yes	Yes	Yes	Yes
Aldec Riviera-PRO (2013.02)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Synthesis</b>							
Synopsys Synplify/Synplify Pro (H-2013.03)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mentor Graphics Precision RTL/Plus (2012c)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Equivalence Checking</b>							
Cadence Encounter Conformal (9.1)	Yes	Yes	Yes	N/A	N/A	N/A	N/A

**Note:** Support for Aldec simulators is offered by Aldec.

**Note:** Contact Synopsys for availability of Synplify Overlay.

**Note:** Cadence Encounter Conformal Support is for RTL2Gate using Synopsys Synplify only.

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## System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

### System Memory Recommendations

For memory recommendations for the ISE Design Suite tools, see:

<http://www.xilinx.com/ise/products/memory.htm>.

### Operating Systems and Available Memory

The Microsoft Windows and Linux® operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs may encounter this limitation. The ISE Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

#### Windows XP Professional 32-bit

Xilinx applications are enabled to take advantage of the memory increase feature on Windows 32-bit systems. You must then modify Windows setting to get access to this larger memory.

The standard Windows OS architecture limits the maximum memory available to a Xilinx process to 2 Gigabyte (GB). In Windows XP Professional, Microsoft created an option to support the ability of an application to address 3 GB of RAM. Xilinx ISE tools have built-in support for this option. To take advantage of this capability, you must also modify your Windows XP OS to enable this feature, which requires that you modify your `boot.ini` file by adding a `/3GB` entry to the end of the `"startup"` line.

Before enabling 3 GB support for Xilinx applications, read the Microsoft Knowledge Base Article #328269 at <http://support.microsoft.com/?kbid=328269>. If you upgrade your computer to Windows XP Service Pack 1 (SP1) and you are using the `/3GB` switch, Windows might not restart without a patch from Microsoft. See the Xilinx Answer Record 17905 for more information at <http://www.xilinx.com/support/answers/17905.htm>.

Additionally, before making this change, read:

- Microsoft Bulletin Q17193 <http://support.microsoft.com/default.aspx?scid=kb;en-us;Q171793>, which contains information on "Application Use of 4GT RAM Tuning".

- Microsoft Bulletin Q289022  
<http://support.microsoft.com/default.aspx?scid=kb;en-us;q289022>, which contains instructions for editing your `boot.ini` file.

## Linux

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the `hugemem` kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site: <http://www.redhat.com/docs/manuals/enterprise/>

## Cable Installation Requirements

Platform Cable USB II and Parallel Cable IV are high-performance cables that enable Xilinx design tools to program and configure target hardware.

To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.

To install Parallel Cable IV, a system must have a parallel port connector and support parallel port communication.

Cables are officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows XP Professional, Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- Root privileges are required.
- SUSE Linux Enterprise 11: The `fxload` software package is required to ensure correct Platform Cable USB II operation. The `fxload` package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.
- Linux LibUSB support: Support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website. See Xilinx Answer Record 29310 at: <http://www.xilinx.com/support/answers/29310.htm>.

For additional information regarding Xilinx cables, see to the following documents:

- USB Cable Installation Guide (UG344):  
[http://www.xilinx.com/support/documentation/user\\_guides/ug344.pdf](http://www.xilinx.com/support/documentation/user_guides/ug344.pdf)
- Platform Cable USB II Data Sheet (DS593):  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds593.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf)
- Parallel Cable IV Data Sheet (DS097):  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds097.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds097.pdf)

## Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

*Table 2-3: Equipment and Permissions Requirements*

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Drive	You must have a DVD-ROM for ISE Design Suite (if you have received a DVD, rather than downloading from the web).
Ports	<p>To program devices, you must have an available parallel, or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable.</p> <p><b>Note:</b> Installation of the cable driver software requires Windows XP Pro SP1 (or later), or Windows-7. If you are not using one of these operating systems, the cables may not work properly.</p>

**Note:** X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

## Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

# Download and Installation

This chapter explains how to download and install the Integrated Software Environment (ISE®) Design Suite tools, which includes ChipScope™ Pro logic analyzer, Embedded Tools (including Embedded Development Kit (EDK) and standalone Software Development Kit (SDK)), System Generator for DSP, and PlanAhead™ design tool.

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## Downloading the ISE Design Suite Tools

This section explains how to download the ISE Design Suite tools.

To begin, open an internet browser and navigate to the Xilinx Download Center at <http://www.xilinx.com/support/download/index.htm>.

Most files in the Xilinx® Download Center are downloaded using the Akamai download manager. For the optimum download experience:

- Allow pop-ups from entitlenow.com
- Set security settings to allow for secure and non-secure items to be displayed on the same page
- Allow the Akamai download manager to run Java processes

To download the Xilinx Design Tools:

1. Select the **Design Tools** tab in the web page.
2. Under the Version heading, click the version of the tools you want to download.
3. Click the link for the installer you want to download.

**Note:** Beginning in 14.3, there is a Multiple File Download option. This option contains four smaller downloadable archives and is the recommended option for customers who cannot reliably download the larger install files. This option requires that all four files listed in the section be downloaded prior to running the installer. See Important Information area of the web page section for more details.

**Note:** For 14.x, the installers under the Xilinx Design Tools heading also contain the standalone selections for the Software Development Kit and Lab Tools. Depending on your use case, you may not need to download these separate installation programs if you are downloading the Xilinx Design Tools installers.

4. Enter your User ID and Password to log into your Xilinx account.

**Note:** If you do not have a Xilinx account, you must create to download products.

An address verification screen appears.

5. After the current address is correct, click **Next**.
6. The Akamai download manager launches in your browser to complete the download process. If you have trouble using the Akamai download manager, look on the download page under "Having Trouble Downloading?". You can follow a link to a Xilinx Answer Record which allows you to obtain the tools without using the download manager.

Most files in the Xilinx Download Center are packaged using TAR methods. You will need to use software from a third party provider to unpack them. Consult your IT department for assistance. Commonly used tools for TAR files are 7-ZIP, GNU built-in tools, WinZIP, and WinRAR. These tools are licensed solely by each respective developer, and not by Xilinx. Xilinx hereby disclaims any warranties, express or implied, including warranties of merchantability, fitness for a particular purpose, or non infringement with respect to these suggested software tools.

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## Installing the ISE Design Suite Tools: Overview for All Platforms

This section explains the installation process for all platforms for the ISE Design Suite tools. Before installation:

- Disable anti-virus software to reduce installation time.
- Make sure you have the necessary privileges for the system on which the design tools will be installed. Some components, such as programming cable device drivers, require administrator-level permissions.
- Close all open programs before you begin installation.
- Make sure your system meets the requirements described in [Chapter 2, Architecture Support and Requirements](#).
- If EDK is installed, make sure the installation is in a directory structure that does not contain spaces.

**Note:** The Xilinx Design Tools installers do not set global environment variables, such as XILINX, on Windows. To find out if this affects the way you run Xilinx design tools, see "[Platform-Specific Installation Instructions](#)."

- When running `xsetup.exe` from a 32-bit machine onto the network location of a 64-bit machine, the tools install the 32-bit executables onto that machine and not the 64-bit executables.

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## Platform-Specific Installation Instructions

This section provides platform-specific instructions for installing the ISE Design Suite tools.

### Microsoft Windows Installation

How you start installation depends on how you obtained the installation program. See [Downloading the ISE Design Suite Tools](#) for details on your options.

- If you downloaded an installation file, decompress that file and run **xsetup.exe**.
- If you downloaded the installation file in multiple parts, decompress the file with the `.tar` extension and run **xsetup.exe**. You should not decompress any other files
- If you received a Xilinx Design Tools DVD, load the DVD. If the auto-run feature of your DVD drive is enabled, the setup program should start automatically. If it does not, browse to the DVD in Windows Explorer and run **xsetup.exe**.

### Linux Installation

The method of starting the installation depends on how you have obtained the installation program. See [Downloading the ISE Design Suite Tools](#) for details on your options.

- If you have downloaded an installation file, decompress that file and run the **xsetup** program contained therein.
- If you downloaded the installation file in multiple parts, decompress the file with the `.tar` extension and run **xsetup**. You should not decompress any other files.
- If you have ordered and received a Xilinx Design Tools DVD, load the DVD. Click the setup file in your file manager, or browse to the root of your DVD drive and type `./xsetup`.

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## Installation Flow

The following section describes important screens you will encounter during the installation process.

**Note:** For each of the following installation steps, click the text of any item with a check box next to it to obtain more information. Information is displayed in the “Description” area near the bottom of the screen.

## Select Download Location Directory

This step applies to users who downloaded the installation files in multiple archive files. If you downloaded a single image, skip to [Accepting Software Licenses](#).

This screen lists all the required additional installation files to complete the installation. Users will need to point the tool to a location that contains these files. All the required files should be in the same directory. After the correct files have been identified, the installer checks the integrity of these files to ensure archives are not corrupt. This process might take a few minutes to complete.

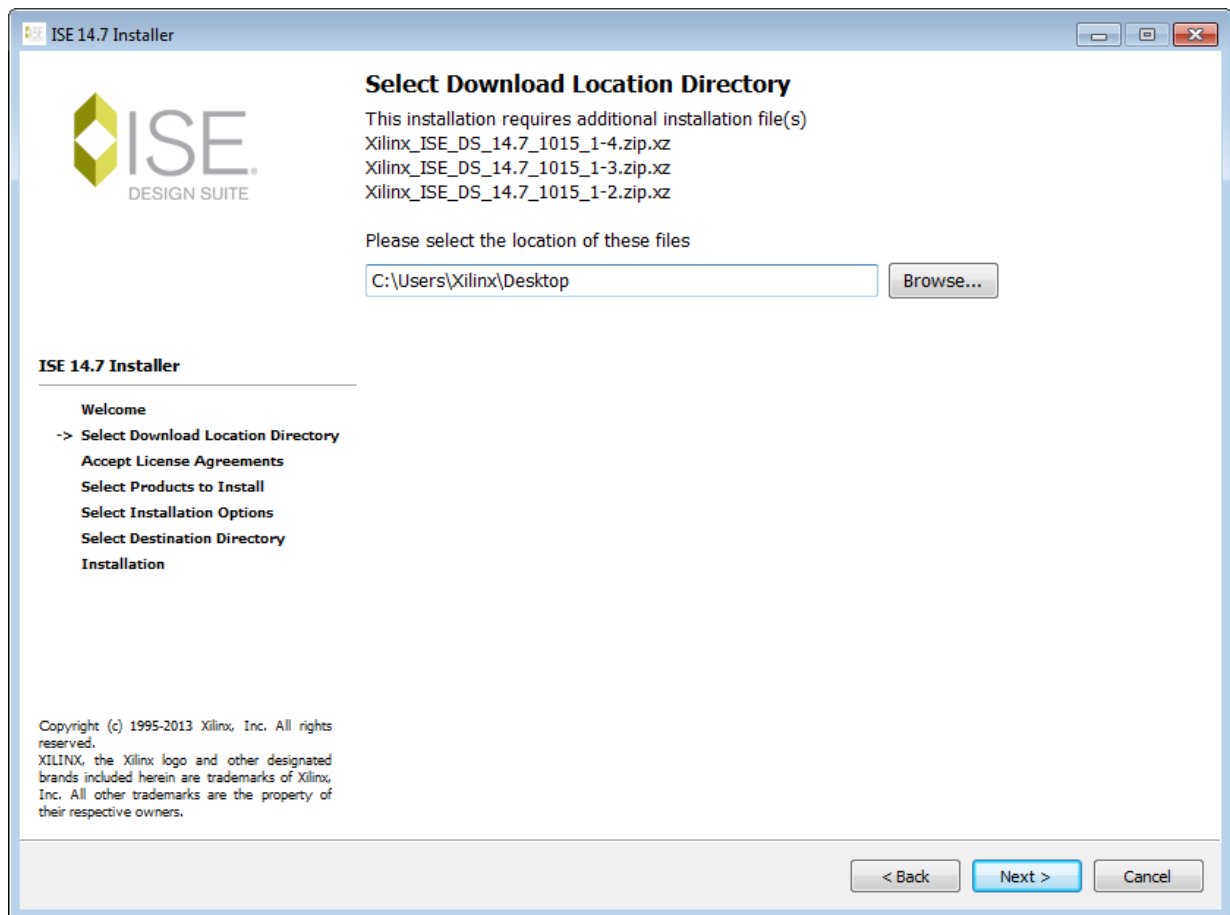


Figure 3-1: ISE Design Suite Tools Installation - Select Download Location Directory

## Accepting Software Licenses

You must accept two software license agreements. On each Accept Software Agreement screen:

1. Click **I accept and agree to the terms and conditions above**.
2. Click **Next**.



## Select Xilinx Products to Install

Select the Xilinx products you want to install.

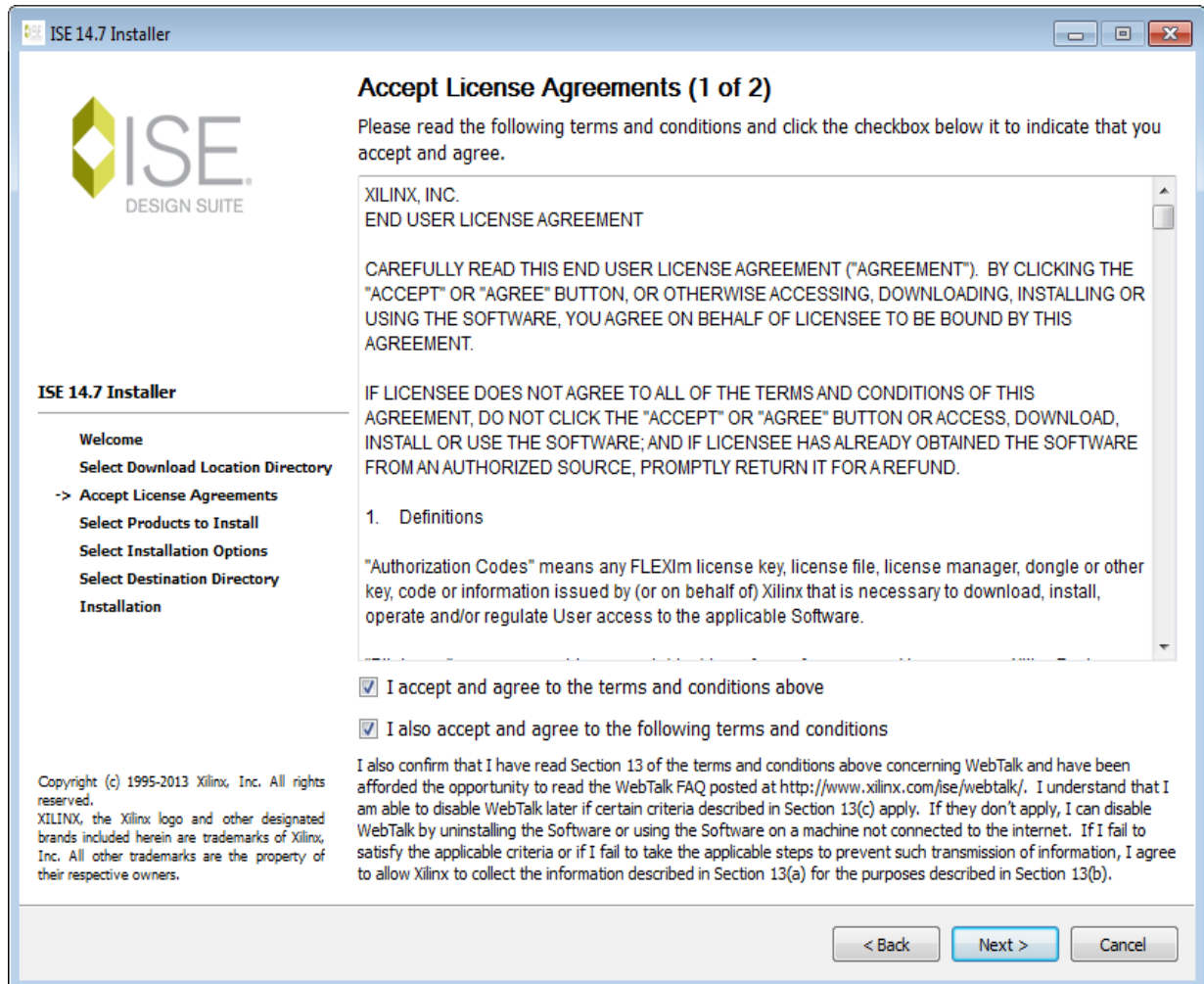


Figure 3-2: ISE Design Suite Tools Installation - Select Xilinx Products Screen

**Note:** The ISE WebPACK™ tool product installer installs both ChipScope Pro analyzer and the Embedded Development Kit. Although installed, these applications will require a separate license to run.

## Select Installation Options

There are several optional installation steps during installation. If selected, these options install toward the end of the installation process, after the main installation has completed.

Select Xilinx Installation Options from the following screen.

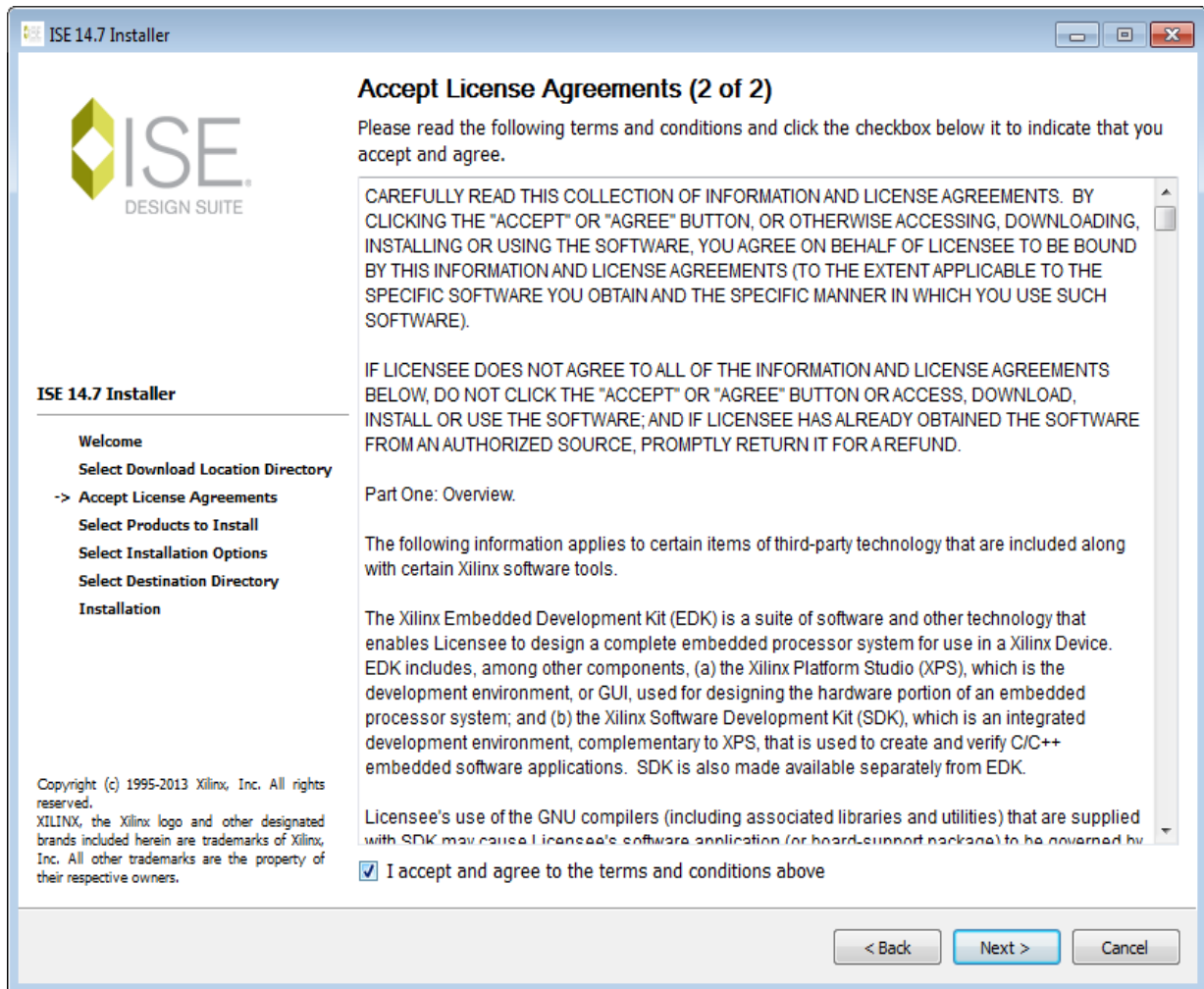


Figure 3-3: ISE Design Suite Tools Installation - Installation Options

**Note:** WebTalk is always enabled when using the WebPACK tool. If you install an Edition product, the installer allows you to deselect Enable WebTalk. However, if a WebPACK tool license is used to process the design, Enable WebTalk is ignored. Click the Enable WebTalk item, in the installer, and read the description box for full details.

## Select Destination Directory

In the Select Destination Directory screen, select the directory in which to install the design tools. Enter a name for the Program Folders list. The installer displays a level of hierarchy underneath the installation path you specify. The name of the directory varies depending on the type of product you are installing. Any Editors or WebPACK tool installation creates a directory named \ISE\_DS. Lab tool standalone installations create \LabTools. SDK standalone installations create \SDK. This ensures Edition and Standalone tools can coexist properly on your hard drive.

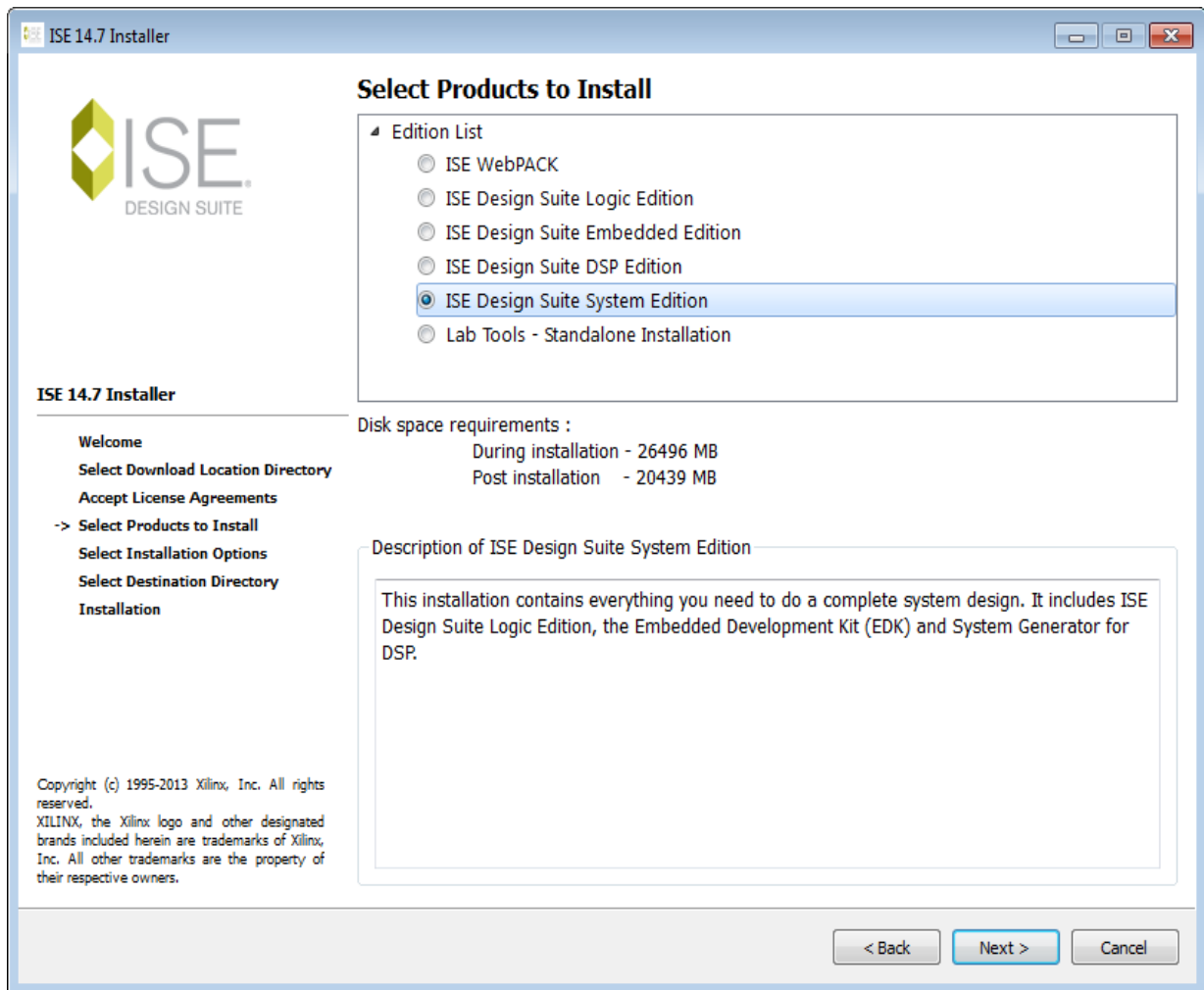


Figure 3-4: ISE Design Tools Suite Installation - Select Destination Directory

## Installation Options Summary

The Installation Options Summary screen summarizes the tools, products, and options to be installed. To begin installation, click **Install**.

Near the end of the installation, the Xilinx License Configuration Manager opens by default. Follow the instructions in the Manager to obtain or locate a license file.

**Note:** EDK tools require the Cygwin tools distributed by RedHat. A copy of these tools is distributed with the EDK installation.

## Setting Environment Variables

### Microsoft Windows Clients

When installation is complete, the installation program creates an environment variable batch file. All appropriate Desktop and Program Group shortcuts call this file before launching the target application. A shortcut to a command-line prompt which sets the environment has been created. The shortcut is located at **Xilinx Design Tools > ISE Design Suite 14.7 > Accessories > ISE Design Suite 32 (or 64) Bit Command Prompt**.

To set environment variables in make or script files:

Add `<XILINX installation directory>\settings32.bat` or `settings64.bat` to your script. The numbers 32 or 64 corresponds to the bit-width of the operating system installed on the computer.

### Linux Clients

When installation is complete, the installation program creates an environment variables file.

1. Go to the XILINX installation directory.
2. Type either `source settings32.(c)sh` or `source settings64.(c)sh`, as required for your shell.

**Note:** 32-bit ISE tools do not work with 64-bit EDK. 64-bit EDK does not work with 32-bit ISE tools.

To set your environment variables manually or from within your setup script, Xilinx recommends you copy the settings from the appropriate file for your operating system, as listed above. Xilinx environment variables settings are specific to each operating system platform.

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## USB FLEXid Dongle Driver Installation

If you purchased a USB FLEXid Dongle for use with the Windows operating systems, you must install the appropriate driver before creating a FLEXnet license for use with it.

1. Install the Xilinx Design Tools first. This installation contains the installer files for the USB FLEXid dongle driver.
2. Run **FLEXid\_Dongle\_Driver\_Installer.exe** from `<Xilinx Installation Directory>\14.7\ISE_DS\ISE\bin\nt`.
3. On the Select Options screen, be sure only **FLEXid 9 Drivers** is checked.

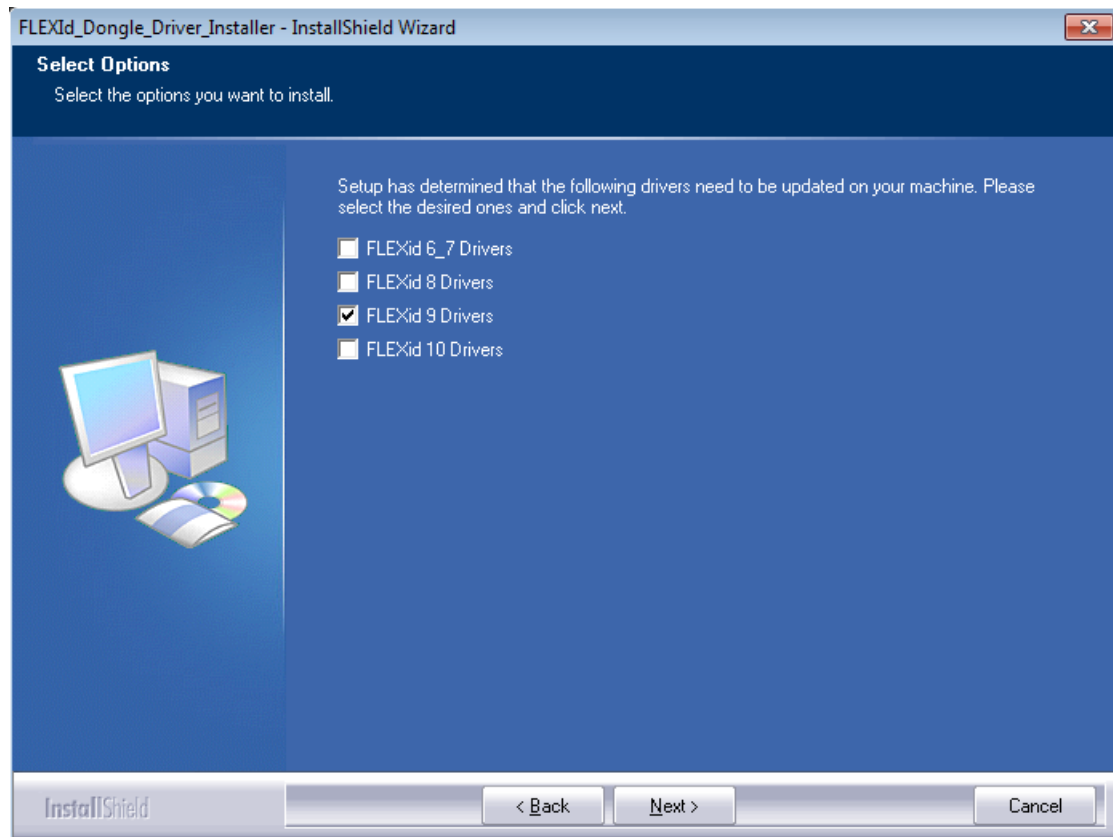


Figure 3-5: Select Options Screen

4. Click **Next** twice. The driver installs.

After installation, you will need to reboot to ensure the dongle operates correctly.

---

## Network Installations

Installing to a network location provides a way for client machines to access the design tools by pointing to it on the network drive. To run the design tools on the network, the client machines must be set up correctly to ensure the environment variables, registry, and program groups all point to the network. The following sections describe the procedure for network setups.

### Linux Clients

Each user must source `settings32.(c)sh` or `settings64.(c)sh` (whichever is appropriate for your operating system) from the \$XILINX area in which the design tools are installed. This points the Xilinx environment variable, path, and LD\_LIBRARY\_PATH to the installed location.

To run the design tools from a remotely installed location, run an X Windows display manager, and include a DISPLAY environment variable. Define DISPLAY as the name of your display. DISPLAY is typically unix:0.0. For example, the following syntax allows you to run the tools on the host named `bigben` and to display the graphics on the local monitor of the machine called `mynode`:

```
setenv DISPLAY mynode:0.0
xhost = bigbenPC Clients
```

## Microsoft Windows Clients

1. Install design tools to a PC network server. Make sure your users know the location of the design tools and have access to the installation directory, and they have Administrator privileges for the following steps.
2. From the local client machine, browse to the following directory:  
`network_install_location\common\bin\nt` and run the program **shortcutSetup.bat**.
3. Running this program sets up the Windows settings batch files and Program Group or Desktop shortcuts to run the Xilinx tools from the remote location.
4. From the client machine, launch the ISE tools by clicking the **Program Group** or **Desktop** shortcuts, or by running the applications on the network drive.

## Installing to a Mounted Network Drive

Xilinx design tools are designed to be installed in a directory under ROOT (typically C:\Xilinx). The installer normally presents this option when installing to a local driver. When installing to a mounted network drive, if a subdirectory is not defined, it appears to the Installer as if it is installing to a ROOT directory.

To work around this issue, define your target installation directory as "`\Xilinx`" under the network mount point (For example: "`N:\Xilinx`").

Windows 7 default security levels do not allow you to select remote mapped drives as an Administrator. To install Xilinx Design Tools on remote mapped drives, you need to change your account control settings using the steps below:

1. Open the Windows Control Panel, from the Windows Start menu, and select 'User Accounts'. If your Control Panel Uses 'Category View', you will need to click 'User Accounts' on two successive screens
2. Click 'Change User Account Control settings' and allow the program to make changes
3. Click and slider the slider-bar down to the second to lowest setting (as seen in the below figure). Click OK.

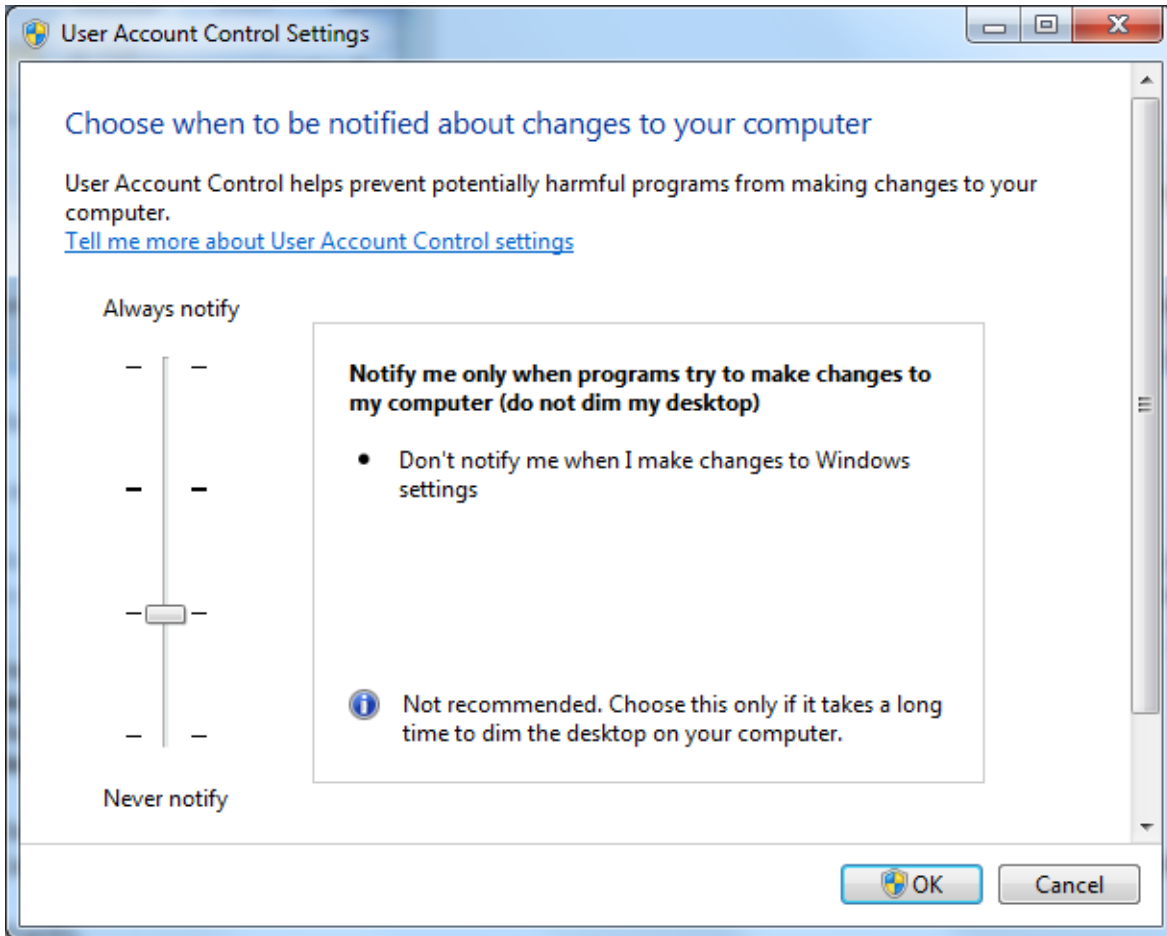


Figure 3-6: User Account Control Settings

Xilinx recommends you revisit this procedure to restore your settings to their previous state after installation.

**Note:** You will not be able to browse to remote mapped drives using the Xilinx installer. You will need to manually type in your installation path which contains a mapped network drive.

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## Obtaining Quarterly Releases

Xilinx releases quarterly versions of the ISE Design Suite tools throughout the year. Each quarterly version contains device support updates, new features and bug fixes. The following sections describe how to obtain updates through XilinxNotify and the Download Center.

## XilinxNotify

The XilinxNotify tool is the preferred method of obtaining updates. It provides the following features:

- Compares the latest version of Xilinx design tools updates available on <http://www.xilinx.com/support> with what you have installed, and notifies you if a newer version is available.
- Provides a Download button allowing you to log in to the Xilinx Download Center. Once you log in, the download of your selected product begins.
- XilinxNotify can be run in any of the following ways:
  - Automatic periodic checks at ISE Project Navigator start-up time.
  - Select **Help > Check for Updates** from Project Navigator.
  - Select **Start > All Programs > Xilinx Design Tools > ISE Design Tools 14.7 > Accessories > Check for Updates**.
  - Type `xilinxnotify` in a Linux shell.

**Note:** Select **Edit > Preferences** in Project Navigator to control the frequency of the automatic periodic checks.

## XilinxNotify Network Installations

By default, the Automatically check for updates option at Project Navigator startup is enabled on the machine used to install the ISE tools to the network location. All clients pointing to this network location have this option disabled by default. Client users have the option of enabling this option (**Edit > Preferences > XilinxNotify** from Project Navigator) and also running manual checks.

**Note:** To perform an update installation, you must have write permissions for the \$XILINX installation directory.

## Download Center

Quarterly releases for all platforms are regularly made available on the Download Center at:

<http://www.xilinx.com/support/download/index.htm>



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# Uninstalling the ISE Design Suite Tools

## Uninstalling on Microsoft Windows

The following sections describe how to uninstall the ISE Design Suite tools on Microsoft Windows.

To uninstall any Xilinx product, select the **Uninstall** item from that product's Start Menu folder. For instance, to uninstall the ISE WebPACK design tools or an ISE Design Suite: Edition, select **Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.7 > Accessories > Uninstall**.

Depending on what you have installed, you may also need to uninstall some ancillary applications, such as WinPcap 4.0 (optional component of DSP Tools).

Before uninstalling, make sure you have moved any project files you want to keep outside your Xilinx installation directory structure, or they will be deleted.

## Uninstalling on Linux

To uninstall the Xilinx Design Suite product, you need to remove the Xilinx installation directory from the shell.

## WebTalk

The WebTalk feature helps Xilinx understand how you use Xilinx® FPGA devices, software, and IP. The information collected and transmitted by WebTalk allows Xilinx to improve the features most important to you as part of our ongoing effort to provide products that meet your current and future needs. When enabled, WebTalk provides information on your use of the ISE® Design Suite tools.

### WebTalk Participation

Your participation in WebTalk is voluntary except in the following cases:

- You are using a WebPack™ license.
- You are using pre-release software or devices.

In these cases, WebTalk data collection and transmission always occurs, regardless of your preference settings. For all other cases, data is not collected or transmitted if you disable WebTalk.

The table below summarizes WebTalk behavior for data transmission to Xilinx from your post-route design, based on your Xilinx license, WebTalk install preference, and user preference settings.

**Table 4-1: WebTalk Behavior for Bitstream Generation or Route Design Flow**

Design Flow	License	WebTalk Install Preference	WebTalk User Preference	WebTalk Data Transmission to Xilinx
Bitstream Generation/ Route Design	WebPACK (or pre-release software)	Ignored	Ignored	Yes (Send)
Bitstream Generation/ Route Design	Logic Edition	Enabled	Enabled	Yes (Send)

**Table 4-1: WebTalk Behavior for Bitstream Generation or Route Design Flow**

Design Flow	License	WebTalk Install Preference	WebTalk User Preference	WebTalk Data Transmission to Xilinx
Bitstream Generation/ Route Design	Logic Edition	Enabled	Disabled	No (Do Not Send)
Bitstream Generation/ Route Design	Logic Edition	Disabled	Ignored	No (Do Not Send)

**Note:** Webtalk transmits data after PAR for devices which bitstream generation is not enabled and after bitstream generation for devices that support bitstream generation.

## Setting WebTalk Install Preference

You can enable or disable WebTalk globally during or after installation as described below. During installation you can enable or disable WebTalk installation options by checking or unchecking the **Enable WebTalk to send software, IP and device usage statistics to Xilinx (Always enabled for WebPACK license)** checkbox.

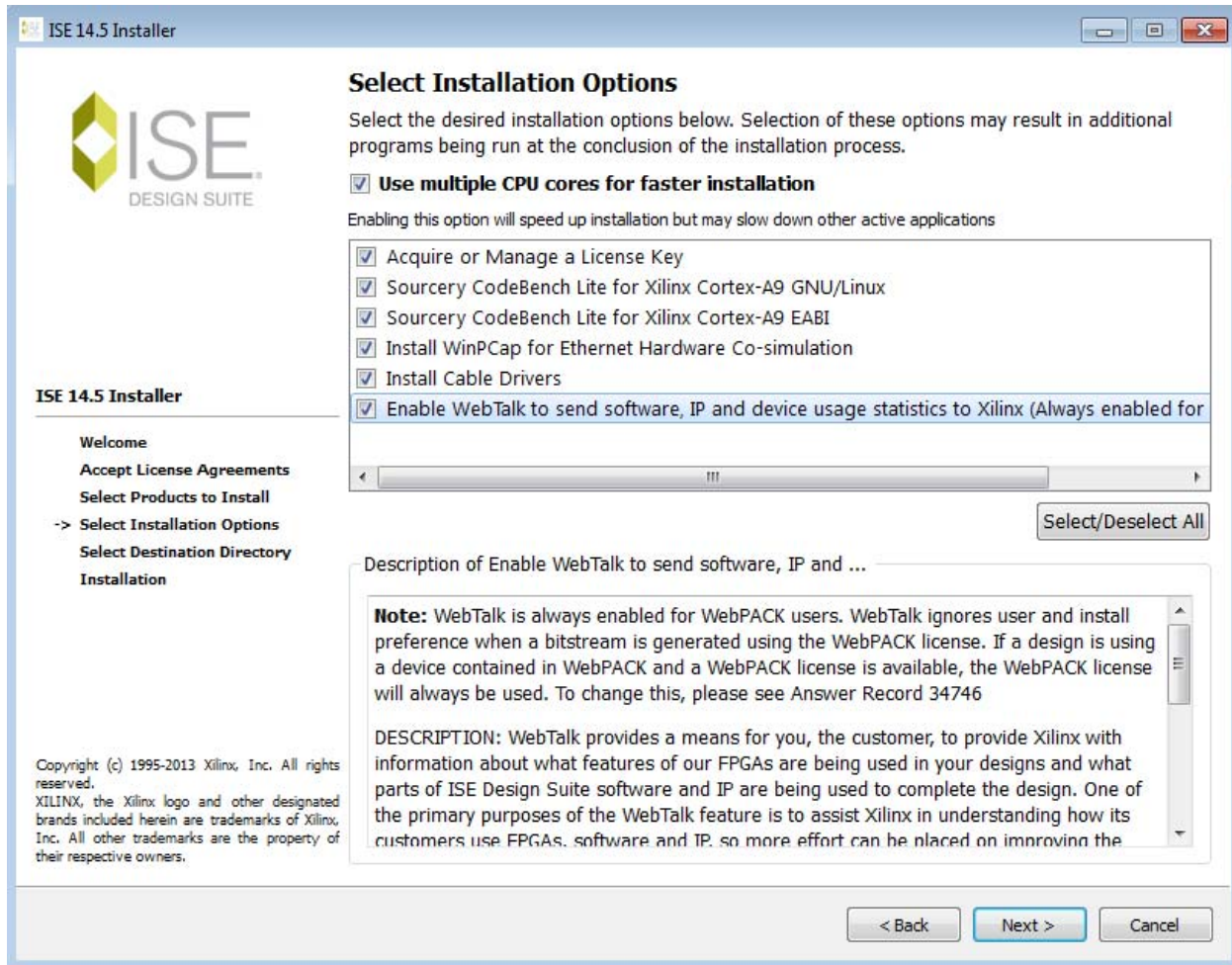


Figure 4-1: WebTalk Install Preference

## Setting WebTalk User Preferences

You can enable or disable WebTalk user options from the Project Navigator Preferences graphical user interface (GUI). For more information, go to the [Xilinx Design Tools WebTalk](#) page available from the Xilinx website.

You can enable or disable WebTalk user options by selecting **Edit > Preferences** as shown below.

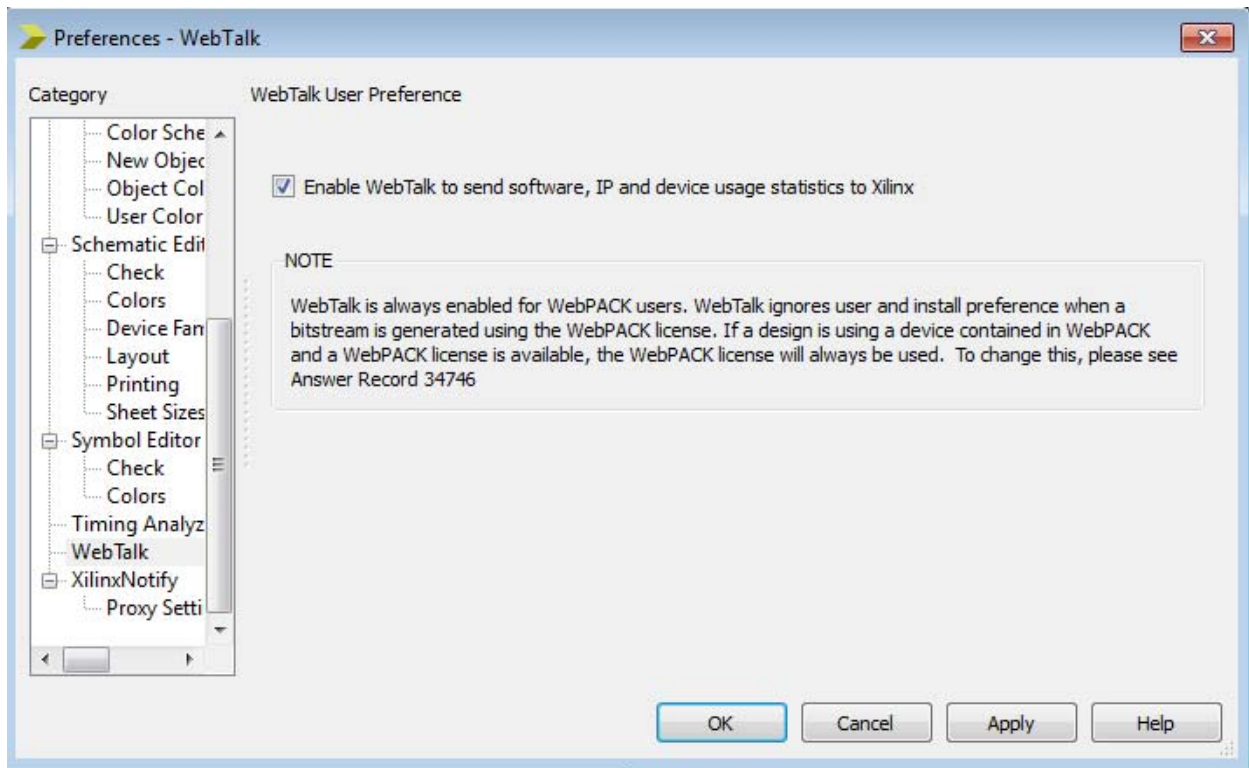


Figure 4-2: WebTalk User Preferences

## Types of Data Collected

WebTalk does not collect your design netlist or any other proprietary information that can be used to reverse engineer your design. The data that Xilinx collects through WebTalk includes:

- Software version
- Platform information (for example, operating system, speed and number of processors, and main memory)
- Unique project ID
- Authorization code
- Date of generation
- Targeted device and family information

For more information on the type of data that is collected, see the [Xilinx Design Tools WebTalk](#) page available from the Xilinx website. To see the specific WebTalk data collected for your design, open the `usage_statistics_webtalk.xml` file in the project directory.

You can also open the `usage_statistics_webtalk.xml` file for easy viewing of the data transmitted to Xilinx.

---

## Transmission of Data

WebTalk is invoked after bitstream or route design compilation. WebTalk bundles the collected data in an `usage_statistics_webtalk.xml` file and sends this file to Xilinx by https (hypertext transfer protocol secure) post. Every new compilation for a given design overwrites the previous `usage_statistics_webtalk.xml` file. WebTalk also writes an HTML file equivalent `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. WebTalk also writes to the `runme.log` file that contains additional information about whether the file was successfully transmitted to Xilinx.

# Obtaining and Managing a License

The Xilinx® Product Licensing Site is an online service for licensing and administering evaluation and full copies of Xilinx design tools and IP products. This chapter describes the FLEXnet license generation functionality of the Product Licensing Site.

---

## Accessing the Product Licensing Site

You can access the Xilinx Product Licensing Site in various ways depending upon the type of license being generated.

- If you purchased products, follow the link included in your order confirmation email. It provides direct access to an account containing your product entitlements.
- To evaluate IP products, go to <http://www.xilinx.com/ipcenter> and follow the Evaluate link on the IP product page of interest.
- To access the Product Licensing Site directly, go to <http://www.xilinx.com/getlicense>. You must first register or enter your registration information.



Sign in to the Xilinx Licensing Site

User ID

Password

[Forgot your password?](#)

Note: Xilinx employees should Sign In using their Xilinx ID and password.

Figure 5-1: Xilinx Licensing Sign In Page

You must first sign in. If you already have a Xilinx user account, enter your user ID and password, and then confirm your contact information is current. If you do not have an account, click the **Create Account** button.

## Changing Xilinx User Account Information

It is important to keep your Xilinx User Account up to date. As you change companies, addresses or emails may change.

### Modifying your Corporate Email Address

1. Go to [www.xilinx.com](http://www.xilinx.com).



Figure 5-2: Xilinx Website

2. Click **Sign In**.



**My Profile**

Please update your profile information by expanding the selections below.

Fields marked with an asterisk \* are required.

- ☐ Personal Information
- ☐ Documentation and Design Advisory Alerts
- ☐ Email Announcements, Updates and Newsletter

Figure 5-3: Personal Information

- Expand **Personal Information**.

## My Profile

Please update your profile information by expanding the selections below.

Fields marked with an asterisk \* are required.

### Personal Information

First Name *	<input type="text" value="Test"/>
Last Name *	<input type="text" value="Xilinx"/>
Corporate Email	<input type="text" value="omsxilinx.test@gmail.com"/>
<i>To change your email address please enter the new address in the field below and select Save Profile. Follow the instructions in the email you receive from us to confirm the change.</i>	
Enter new Corporate email address	<input type="text"/>
<a href="#">Change password</a>	
Company/Organization	<input type="text" value="xilinx oms"/>
Address 1	<input type="text" value="3100 Logic Dr"/>
Address 2	<input type="text"/>
City	<input type="text" value="Longmont"/>
State/Province	<input type="text" value="CO"/>
Postal/Zip Code	<input type="text" value="80503"/>
Country	<input type="text" value="United States"/>
Phone (include area code)	<input type="text" value="7206523211"/>
Fax (include area code)	<input type="text"/>
Preferred Language	<input type="text" value="English"/>
Job Function	<input type="text" value="Other"/>
Industry *	<input type="text" value="Other"/>

[Documentation and Design Advisory Alerts](#)

[Email Announcements, Updates and Newsletter](#)

Figure 5-4: Enter New Corporate email Address

4. Enter your new corporate email address in the **Enter new Corporate email address** box.
5. Click **Save Profile** button for changes to take effect.

## Product Licensing Accounts

When you purchase a design tool edition or IP product from Xilinx, you are purchasing a license to use and receive updates for that product for one year. The license to use Xilinx design tools and IP products is managed through the use of product entitlements. A product entitlement is the determination of:

- Which product was purchased
- The number of seats purchased
- The license type (floating or node-locked)
- The product subscription period (product updates are provided throughout the year)

In addition to managing the product entitlements for your purchased design tools and IP, you can also access product entitlements for No Charge or Evaluation products. Full and No Charge licenses have a subscription period of one year. Design tools evaluations are for 30 days, and IP evaluations are for 120 days.

Activating a product entitlement results in one or more license keys being generated by the website. When installed, the license keys enable the use of the design tools and IP that were purchased or are being evaluated. Your product entitlements and resulting license key files are managed in a product licensing account on the Xilinx website.

Product licensing accounts are specific to the individual listed on the Xilinx Software Purchase Order, who is either the end user or administrator of the design tools. All purchases made can be managed in the same product licensing account if a single administrator is named. A company site can have multiple accounts managed by different administrators. The latter is helpful if a site has multiple design teams working on differing projects with different budget pools.

**Note:** A license key can be generated for a product entitlement that has expired; however, it will only enable product releases up to the subscription end date. Applying a product update made available after the subscription end date of your license results in an error.

## LogiCORE IP License Generation

Any LogiCORE™ IP and design tools entitlements you have purchased appear in your list of entitled products when you log into the Product Licensing Site. Licenses for Evaluation and No Charge IP are available on the site in a separate area. Licenses for all your design tools and IP can now be generated in one pass. They are emailed to you in a single license file. IP core FLEXnet licenses now feature more licensing options, such as single or Triple-Redundant Floating Server support, and more host options for node-locked license keys: Ethernet MAC address, Hard Drive Serial Number or USB Dongle ID.

---

## User Types and Actions

There are three user types for the Product Licensing Site: customer account administrator, end user, and evaluation user.

### Customer Account Administrator

An example of a typical customer account administrator is a CAD tools manager. Every product licensing account *must* have at least one customer account administrator. A customer account administrator can manage more than one product licensing account.

The responsibilities as the customer account administrator include:

- Generating node-locked or floating licenses for Xilinx design tools and IP products.
- Adding and removing users from the product licensing account.
- Assigning administrative privileges to other users.
- Ordering product DVDs (if desired).

The original customer account administrator is the Ship To contact identified during the product ordering process. That person receives an email with instructions on how to download and license each purchased product. The customer account administrator must follow the link in the email, to ensure access to the purchased products.

### End User

Adding end users to a product licensing account allows an engineer or design team member the flexibility to manage and generate license keys on their own. The end user may generate license keys for node-locked products entitlements within the account as well as evaluation and “no charge” license keys for design tools and IP products. A customer account administrator can also configure the end user account to allow an end user to generate floating licenses. An end user cannot:

- View or generate floating license keys by default. This privilege may be assigned to them by the customer account administrator.
- View the license keys generated by other users.
- Add or remove other users to or from the product licensing account.

### Evaluation User

Evaluation users can:

- Generate a 30-day free evaluation license key for the Vivado Design Suite: System Edition which includes the ISE® Design Suite: System Edition
- Generate license keys for evaluation and no charge IP products
- Generate a WebPACK™ tool license for the Xilinx Design Tools
- Request a Xilinx Design Tools DVD package with one of the following shipping options:
  - Free Shipping (2-4 Weeks)
  - Standard (2-3 Days)
  - Overnight

**Note:** A customer who is already licensed for a full version of a Xilinx Design Tools product edition can evaluate other Xilinx Design Tools product editions or IP. These product entitlements are made available in the same product licensing account.

All user types can download products electronically and request a Xilinx Design Tools DVD.

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## Creating a License Key File

The Create New Licenses tab on the Product Licensing Site is the starting point for license key file generation. The design tools and IP product entitlements you have purchased or wish to evaluate are shown in the product entitlement table.

Home : [Support](#) : Product Licensing

## Product Licensing

Account: Xilinx Test Account - 10101

[Create New Licenses](#)
[Manage Licenses](#)
[Legacy Licensing](#)
[Orders](#)
[Manage Users](#)
[Restricted Downloads](#)

**Have a Voucher to Redeem?** [?](#)

xxxx-xxxxxx-xxxx-xxxxxx

enter voucher code

[Redeem Now.](#)

**Evaluation and No Charge Cores** [?](#)

Search the **Evaluation and No Charge** cores catalog and add specific cores to table below

[Search Now.](#)

**Create a New License File for Account: Xilinx Internal**

Create a new license file by making your product selections from the table below. Floating and Node-Locked licenses cannot be combined in the same license file. [?](#)

Product	Type	License	Available Seats	Status	Subscription End Date
<input type="checkbox"/> Petalinux SDK Evaluation License (No Support)	Evaluation	Node	1/1	Current	365 days
<input type="checkbox"/> Vivado and ISE Design Suite: WebPACK License	No Charge	Node	1/1	Current	None
<input type="checkbox"/> Vivado and ISE Design Suite: 30-Day Evaluation, Node-Locked License	Evaluation	Node	1/1	Current	30 days
<input type="checkbox"/> Vivado HLS Evaluation License	Evaluation	Node	1/1	Current	30 days
<input checked="" type="checkbox"/> Vivado/ISE Design Suite: System Edition, Floating License	Full	Floating	18/20	Current	02 Aug 2011

[Generate Floating License](#)
[Generate Node-Locked License](#)

Figure 5-5: Create New License

## Selecting Products

To begin the license generation process for products you have purchased or want to evaluate:

1. Select a product licensing account from the Account drop-down list.  
**Note:** This selection is not available if you are entitled to evaluation or free products only.
2. Enter product voucher codes for design tools or IP product licenses purchased with kits or for tools purchased from the Xilinx online store (optional).
3. Add evaluation or no-charge IP product entitlements to the product entitlement table (optional).
4. Make your product selections from the product entitlement table.

The type of product entitlements available are Full (purchased), No Charge, or Evaluation. Full and No Charge licenses have a subscription period of one year. Design tools evaluation is for 30 days. IP evaluations are for 120 days.

Floating and node-locked licenses cannot be combined in the same license key file.

**Note:** A floating license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased. A node-locked license allows for the use of a single seat of a product entitlement on a specific machine.

For design tools, available seats represents the number of seats available for licensing over the total number of seats purchased. For IP, seats are managed according to the terms of the site wide license agreement.

Products with a status of Current are within their warranty period. Products with a status of Expired have a warranty period end date that has passed. If seats are available, licenses can be generated for either Current or Expired product entitlements.

The Xilinx Design Tools: System Edition evaluation product entitlement provides access to all the capabilities in the Xilinx Design Tools tool set. This product entitlement is automatically included in your product licensing account.

Product vouchers for design tools and IP product licenses may be shipped with a Xilinx or partner development board or design kit. If you have a product voucher card, you may enter the voucher code on the card into the associated text field and click Redeem Now. This places the corresponding design tools or IP product entitlement in the product entitlement table which you can use to generate a license key.

To add Evaluation and No Charge IP to the list of product entitlements, click the **Search Now** button in the Add Evaluation and No Charge IP Cores section of the page. This opens an IP product finder tool.

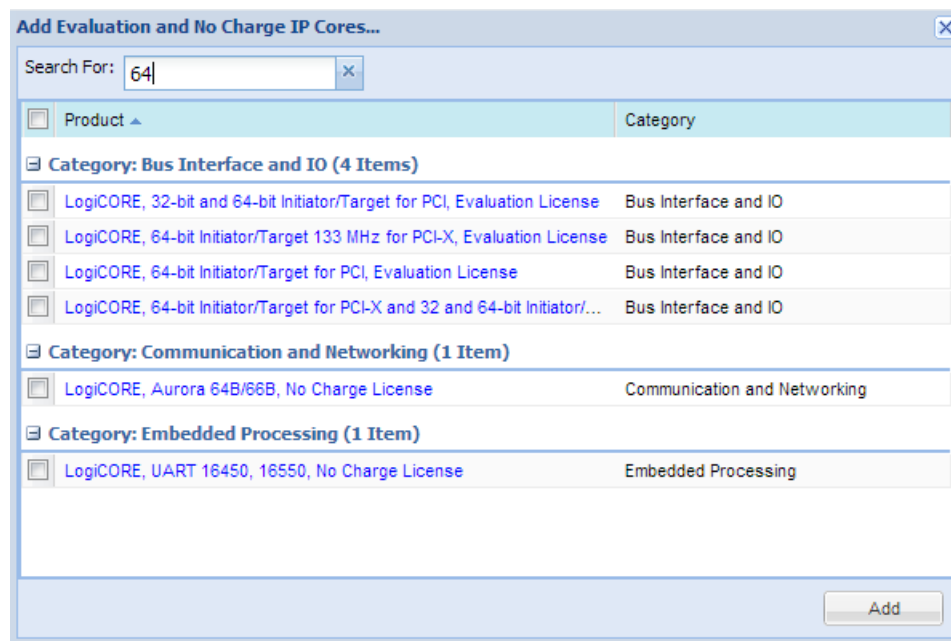


Figure 5-6: IP Product Selector

**Note:** IP products are typically sold as site licenses that gives the administrator the ability to generate license keys for floating and node-locked license types. End users see only product entitlements for node-locked products. The customer account administrator, or an End User who has been granted Floating License generation status by the administrator, sees product entitlements for both node-locked and floating products.

## Generating a License

Click the **Generate License** button corresponding to the type of license key file you are generating (floating or node-locked). The license generation form shown below appears.

### Generate Floating License

*Fields marked with an asterisk \* are required.*

#### 1 PRODUCT SELECTION

Product Selections *	Product	Type	Available Seats	Subscription End Date	Requested Seats
<input checked="" type="checkbox"/>	Vivado/ISE Design Suite: System E...	Full	189/200	01 AUG 2013	<input type="text" value="10"/>

#### 2 SYSTEM INFORMATION

License: Floating

Redundancy [?](#)
☒ Non-Redundant
☐ Triple Redundant

Host ID [?](#)

#### 3 COMMENTS

Comments [?](#)

Figure 5-7: Generate Floating License

To generate floating licenses:

1. Select the number of seats required for each product license.



This is for floating licenses only. All node-locked licenses are for one seat. The number of seats available for a product entitlement is automatically maintained by the system. The Requested Seats field is populated, by default, with the full number of seats remaining on the product entitlement. A product is removed from the product entitlement table if all seats have been activated.

2. Enter system information.

System information is pre-populated in the option menu if you arrived at the Product Licensing Site from a link within the Xilinx License Configuration Manager (XLCM).

A redundant server configuration provides a fail over for the license manager software. As long as two of the three servers are running, the license manager can continue to run.

If you do not have pre-populated system information, or if you want to add a different host, select the **Add a host** option.

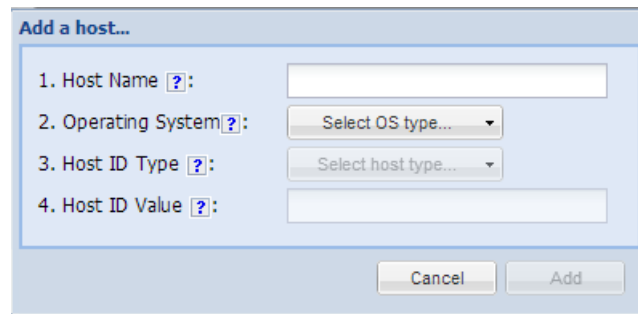


Figure 5-8: Add a Host

The host ID value uniquely identifies the machine to which your design tools or IP is licensed. You may choose a host ID type to be a MAC address, a hard drive serial number, a dongle ID, or a Solaris host ID.

**Note:** Not all host ID types are supported for all operating systems. The easiest way to obtain your host ID is to run the XLCM on the machine that serves as the license host.

3. Add a comment.

Adding a comment to the license key file makes it easier for an administrator to track the allocation of design tools and IP product entitlements among users.

4. Click **Next**.

The Review License Request form opens.

**Generate Floating License**

**4 REVIEW LICENSE REQUEST**

**Product Selections**

Product	Subscription End Date	Available Seats	Requested Seats
Vivado/ISE Design Suite: System Edition/DSP Edition, ...	2013-08-01	18/20	10

**System Information**

License	Floating
Redundancy	No
Host Name(s)	TestHost
Host ID	12345678ABCD

Note: WebTalk is always enabled for WebPACK users. WebTalk ignores user and install preference when a bitstream is generated using the WebPACK license. If a design is using a device contained in WebPACK and a WebPACK license is available, the WebPACK license will always be used. To get additional information on WebTalk, go to [www.xilinx.com/ise/webtalk](http://www.xilinx.com/ise/webtalk).

Previous Next Cancel

Figure 5-9: Review License Request

5. Review your selections.
6. If you are satisfied with your selections, click **Next**.

## End User License Agreements

Xilinx Design Tools and No Charge IP product End User License Agreements (EULAs) are agreed to during the product installation process. If you license IP products, you must accept the terms of the associated IP product EULAs before the license file can be generated.

## Third-Party Licenses

A complete copy of the third-party licenses is located at:  
`<install_directory>/common/licenses/unified_3rd_party_eula.txt`

## License Generation Confirmation

When you finish generating the licenses, you will receive a confirmation message summarizing your licensing activity.

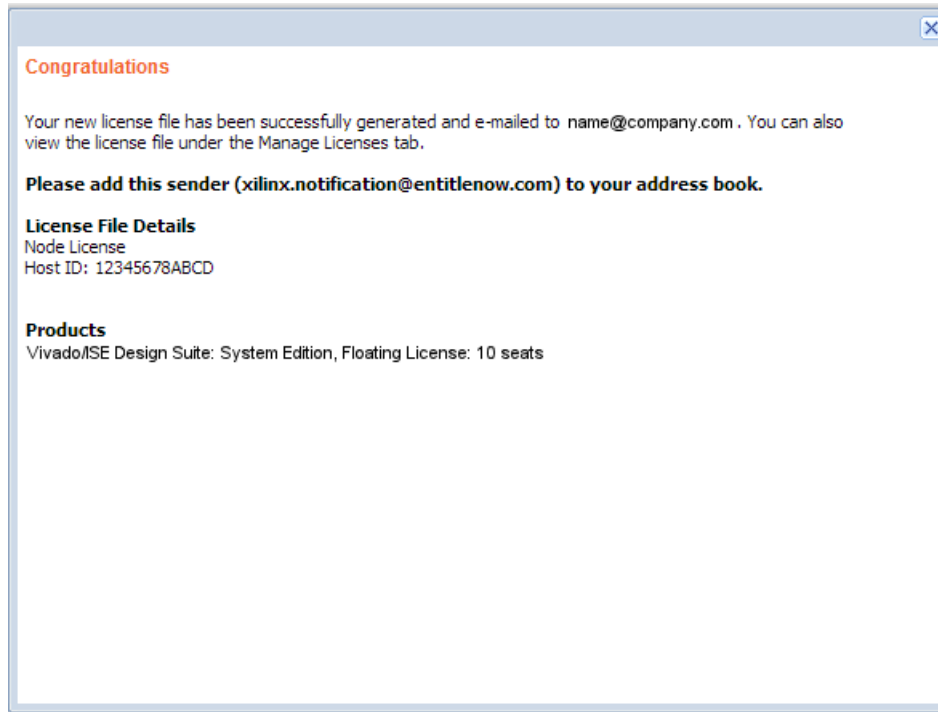


Figure 5-10: License Generation Confirmation

You will also receive a license generation confirmation email. This message contains the generated license key file as an attachment. Add 'xilinx.notification@entitlenow.com' as a trusted sender in your email address book.

If you do not receive your license by email, you can download it directly from the Xilinx Licensing Site. See the [Managing License Key Files](#) section for details

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## Managing License Key Files

The Product Licensing Site tracks your license key files. Select the Manage Licenses tab to see all license key files for your product licensing account.

Home : [Support](#) : Product Licensing

## Product Licensing

Account: Xilinx Test Account - 10101

[Create New Licenses](#)
[Manage Licenses](#)
[Legacy Licensing](#)
[Orders](#)
[Manage Users](#)

Manage License Files for Account: Xilinx

Host Name	Host Type	Host ID	License Type	OS	Created By	Created Date
TestHost	Ethernet MAC	12345678ABCD	Node	Windows 64-bit	JOHN SMITH	16 MAR 2013
JSMITH1	Disk Serial Number	99999999	Node	Windows 32-bit	JANE SMITH	06 DEC 2011
JSMITH2	Ethernet MAC	DCBA87654321	Node	Windows 32-bit	JANE SMITH	16 DEC 2010

TestHost	12345678ABCD	Node	RAYMOND MARTIN	16 MAR 2013										
Comments	<table border="1"> <thead> <tr> <th>Product</th> <th>Type</th> <th>Status</th> <th>Subscription End Date</th> <th>Activated Seats</th> </tr> </thead> <tbody> <tr> <td>Vivado and ISE Design Suite: System Edition, Node-Locked License</td> <td>Full</td> <td>Current</td> <td>30 Jun 2013</td> <td>1</td> </tr> </tbody> </table>				Product	Type	Status	Subscription End Date	Activated Seats	Vivado and ISE Design Suite: System Edition, Node-Locked License	Full	Current	30 Jun 2013	1
	Product	Type	Status	Subscription End Date	Activated Seats									
Vivado and ISE Design Suite: System Edition, Node-Locked License	Full	Current	30 Jun 2013	1										

[Modify License](#)

Figure 5-11: Manage Licenses

Use the Manage Licenses page, to perform the actions described below.


## Exploring and Retrieving Your Existing License Key Files

Information regarding the license key files in your product licensing account are displayed in a split-section view. Click a row in the master view in the top table, to see detailed information about the license key file in the detail view in the bottom table. The detail view table displays:

- A list of product entitlements activated in the key file.
- Comments associated with the key file.

The detail view table gives you the ability to:

- Download - If your license file does not arrive via email you may download the license file here.
- Email - The license file may be emailed to you or another user.
- View - Gives you the ability to view the actual license file.

- Delete - Delete the license file. Once a file is deleted it will then become available on the Create New License page and may be regenerated for another host ID. 
- View the end user license agreement (IP only).

## Modifying a License Key File

To modify an existing license key file, select the license key file in the master view. You can modify a license key file as follows:



### Delete an entire license file and place entitlement back into your account

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file you wish to delete.
2. Click the **Trash Can** icon located below and to the left of the license file details.
3. Click the **Accept** button to accept the Affidavit of Destruction.

**Note:** This will delete all license seats in the entire license key file and return the entitlements to your account.

### Rehost or change the license server host for a license key file

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file you wish to rehost.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **System Information**.
4. Change or add new Host ID and/or Host Name by using the drop-down list and text entry boxes respectively.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

### Activate or add additional seats to an existing licensed product entitlement

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file to which you wish to add seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and add seats up to the total number of seats available in your entitlement.
5. Click **Next** twice. No Affidavit of Destruction is required for adding seats.

## Deactivate or remove seats from an existing licensed product entitlement

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file from which you wish to remove seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and reduce the number of seats that will be authorized by this license file.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

## Activate or add additional product entitlements to a license key file

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any new entitlements you wish to add to this license file.
5. Click **Next** twice. No Affidavit of Destruction is required for adding features.

## Deactivate or delete product entitlements from a license key file

1. From the Manage Licenses Tab (see [Figure 5-11](#)), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any entitlements you wish to remove from this license file.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

Modifying a key file uses the same input form as when the license key file was created, except additional product entitlements of the same license type (floating or node-locked) are made available for licensing.

If, during any of the modification steps, you receive a message that you have exceeded your number of rehost attempts, email [cs\\_1@xilinx.com](mailto:cs_1@xilinx.com) to request additional rehost options.

## Reclaiming Deactivated Product Entitlements

A product entitlement is deactivated when one of the following occurs:

- Rehosting or changing the license server host for a license key file.
- Deactivating or removing seats from an existing licensed product entitlement.
- Deactivating or deleting product entitlements from a license key file.

The license generation facility allows the reallocation of the deactivated seats or product entitlements by making the corresponding seats or product entitlements available for activation in the product entitlements table on the Create License page.

Before the reallocation of entitlement occurs, you must first agree to an Affidavit of Destruction. This legal agreement is required to ensure the deactivated product entitlements are no longer being used.

The number of allocation operations is recorded for each user. Administrators are allowed to reallocate product entitlements five times per major release. End users are allowed to reallocate product entitlements three times per major release.

## What Happens to Your License Key File

For each product entitlement activated, a FLEXnet increment line and corresponding package line is added to the license key file. When a license key file is modified to activate (add) seats for an existing or new product entitlement, additional increment or package lines are added to the license key file.

When a license key file is rehosted or is modified to deactivate (delete) seats or product entitlements, the corresponding increment lines are regenerated or removed from the modified license key file.

---

## Legacy Licensing

If you wish to obtain a license for Releases 10.1 or earlier, click the **Legacy Licensing** tab.



Figure 5-12: Legacy Licensing

Then complete the following steps for the respective versions:

## 10.1 and Prior Versions

1. Select the version you desire. You will be prompted to verify your contact information.
2. Fill out the requested form with the required information to receive your registration IDs. Your registration ID will be displayed on the screen and emailed for your records.
3. Go to the Xilinx download center, click the **Archive** link under the **Version** column on the left side of the page to select the product you desire.
4. During the download process you will be prompted to insert your registration ID to complete the download process.

---

## Understanding Your Tool and IP Orders

The Orders tab will display information regarding the purchasing orders that created the entitlements you see in this account.



The screenshot shows the Xilinx web interface with the 'Orders' tab selected. The interface is divided into two main panels. The left panel, titled 'Orders', contains a table with columns: Date, Order Number, State, and Line Items. The right panel, titled 'Order Details', shows information for a selected order (Order #: 3372646-2). Below the order details, there are two sub-sections: 'Billing Information' and 'Shipping Information'.

Date	Order Number	State	Line Items
01/05/2011	AX-ON-1294239675909	COMPLETED	1
11/23/2010	AX-ON-1290534591370	COMPLETED	1
04/18/2010	AX-ON-1271608207513	COMPLETED	1
12/12/2009	AX-ON-1260636434533	COMPLETED	1
06/04/2009	3372646-2	COMPLETED	1
06/04/2009	3372646-1	COMPLETED	1
06/04/2009	3372646-4	COMPLETED	1
06/04/2009	3372646-3	COMPLETED	1

**Order Details**

Order #: 3372646-2  
 Date: 06/05/2009 12:00:00  
 State: COMPLETED  
 Warranty Start: 04/08/2009  
 Warranty End: 04/30/2010

Line	Quantity	Sku	Description
2	1	0451118	LogiCORE, 32-bit and 64-bit Initiator/Targe...

**Billing Information**

First Name:  
 Last Name:  
 Email:  
 Address 1:  
 Address 2:  
 City:  
 State:  
 Postal Code:  
 Country:

**Shipping Information**

First Name: KRISTIN  
 Last Name: PERRY 222701  
 Email:  
 Address 1: 3100 LOGIC DRIVE  
 Address 2:  
 City: LONGMONT  
 State: CO  
 Postal Code: 80503  
 Country: US

Page 1 of 1  
 Displaying 1 - 8 of 8

Figure 5-13: Order Information

- Xilinx order numbers are listed on the left panel of the screen.
- Order details populate on the right panel of the screen when you highlight specific order.
- You may only select one order at a time.
- The order's shipping address information is visible even when product is delivered electronically.

## Managing User Access to Product Licensing Account

The responsibility of administering a product licensing account may be transferred or shared with another user. The ability to add or remove users from a product licensing account is managed under the Manage Users tab.

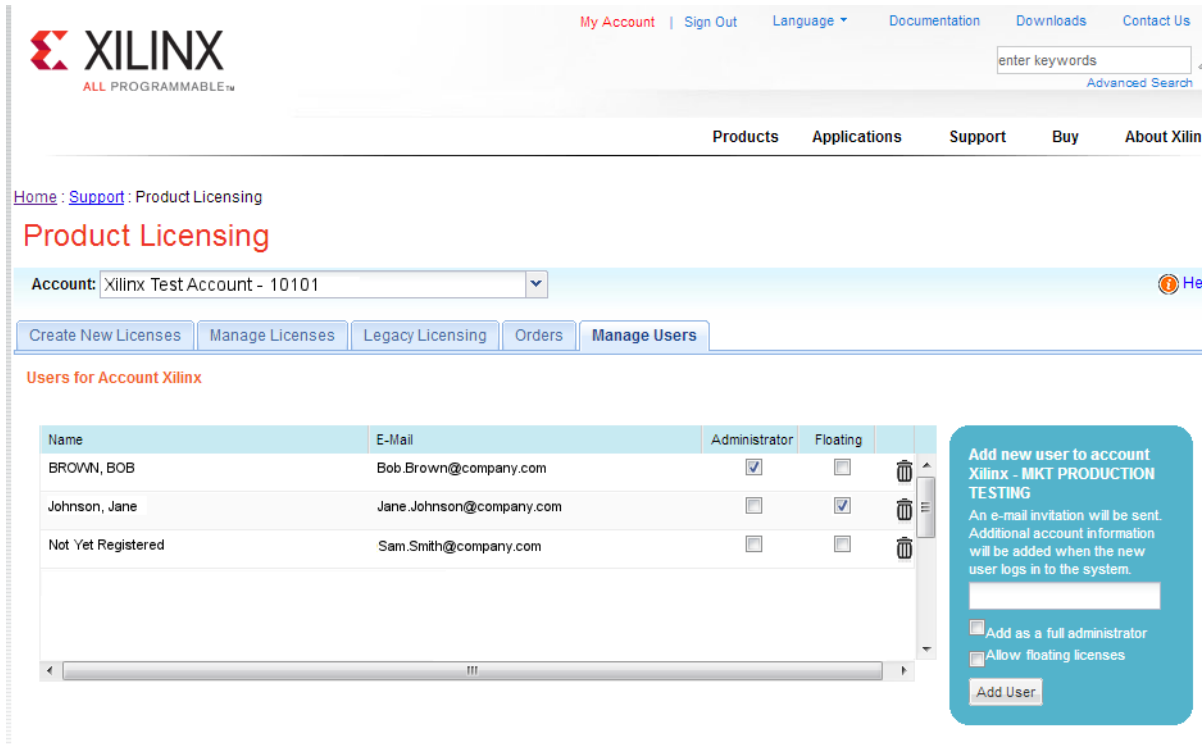


Figure 5-14: Manage Users

## Adding Users

To add a user to your product licensing account:

- Type in the corporate email address of the new user.
- Check **Add as a full administrator**, to grant the new user customer account administrative privileges. Check **Allow Floating Licenses**, to grant the new user the ability to generate Floating Licenses, but not have full administrative privileges.

**Note:** The email address you provide must be the same email address the user supplied or supplies when creating their Xilinx account. If not, you may not be properly recognized when logging in.

If you have already logged into the Product Licensing Site, your name appears in the user list. If the user has never been to the site, the words Not Yet Registered appears in the space for their name. Once the user has signed in, their name is filled in.

In some instances, a customer account administrator may wish to have design team members administer license key files for their own use. By leaving both Add as full administrator and Allow Floating Licenses check boxes unchecked, the user is granted the following restricted privileges:

- Can generate node-locked license keys only.
- Can view and modify only those license key files they generated for themselves.

- Cannot manage users.

If you check Allow Floating Licenses only, the restriction on node-locked keys is lifted, but the others remain. You cannot check both boxes because it is not allowed. Full administrators already have floating license generation capability.

## Removing Users

To remove administrative or floating license generation privileges from a user, uncheck the **Administrator** or **Floating** check box for that user.

To remove a user from a product licensing account, click the **Trash Can** icon for that user.

---

# Installing Your License Key File

The following subsections describe installing different types of licenses.

## Node Lock License Installation

After generating a license file, you will receive an e-mail from 'xilinx.notification@entitlenow.com'.

1. Save the license file attached to the e-mail to a temporary directory on your local system.
2. Run the Xilinx License Configuration Manager:
  - For Windows: Select **Start > All Programs > Xilinx Design Tools 14.7 > Accessories > Manage Xilinx Licenses**.
  - For Linux: Type **xlcm** in a command-line shell.
3. Click **Copy License** at the top of the Manage Xilinx Licenses tab.
4. Browse to your license file (`xilinx.lic`) and click **Open**.
5. This copies the license file to the `C:\.Xilinx` (Windows) or `<Home>/ .Xilinx` directory of your computer where it will be automatically found by the Xilinx tools.
6. When the Copy License operation is complete, the table on the Manage Xilinx Licenses tab is updated with licensing information from the license file.
7. Click **Close** to exit the Xilinx License Configuration Manager.

## Floating License Installation on Servers

For existing FLEXnet license servers, a common practice is to copy the contents of the license file, mailed from 'xilinx.notification@entitlenow.com', into the existing license file on your FLEXnet server.

**Note:** Restart the floating license server to enable the Xilinx licenses.

### For New License Servers

1. Download the appropriate Xilinx FLEXnet license utilities for your server's operating system from the Xilinx Download Center:

<http://www.xilinx.com/download/index.htm>

2. Unzip these utilities into a destination directory. Xilinx recommends you place this directory into your application search path.
3. Once the FLEXnet utilities are installed, run the following commands to start the floating license server:
  - Linux
    - <Server Tool directory>/bin/linux/lmgrd -c <path\_to\_license>/Xilinx.lic -l <path\_to\_license>/log1.log
    - <Server Tool directory> bin/linux64/lmgrd -c <path\_to\_license>/Xilinx.lic -l <path\_to\_license>/log1.log
  - Windows
    - < Server Tool directory>\bin\nt\lmgrd -c <path\_to\_license>\Xilinx.lic -l <path\_to\_license>\log1.log
    - < Server Tool directory>\bin\nt64\lmgrd -c <path\_to\_license>\Xilinx.lic -l <path\_to\_license>\log1.log

## Client Machines Pointing to a Floating License

1. Run the **Xilinx License Configuration Manager (XLCM)**.
2. Click the **Manage Xilinx Licenses** tab.
3. On the Manage Xilinx Licenses tab, enter the network path to the license server in the port@server format into the XILINXD\_LICENSE\_FILE field. Click **Set**. The default Xilinx port number is 2100.
4. For Linux operating systems, licensing environment variables cannot be set using the Xilinx License Configuration Manager (XLCM). The environment variable fields are read only, and they are grayed out and there are no Set buttons. The environment variable must be set using the appropriate shell and commands.

# Technical Support and Documentation

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## Known Issues

ISE® Design Suite Tools Known Issues can be found at the following Xilinx® Answer Record: <http://www.xilinx.com/support/answers/46491.htm>.

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## Support Site

For general technical questions, visit the Xilinx Product Support and Documentation site at <http://www.xilinx.com/support/>, where you can search the Answers Database or utilize other self-support features such as:

- Download Center, <http://www.xilinx.com/support/download/index.htm>
- Xilinx User Community Forums, <http://forums.xilinx.com>
- Free Design Training Videos, <http://www.xilinx.com/training/free-video-courses.htm>

If you cannot resolve your issue using our online resources, you can contact Xilinx Technical Support directly at <http://www.xilinx.com/support/techsup/tappinfo.htm>.

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## Customer Training

Xilinx hands-on training programs provide you with the foundational knowledge necessary to begin designing right away. These programs target both engineers new to FPGA technology and experienced engineers developing complex connectivity, digital signal processing, or embedded solutions.

For more information on training courses, free on-demand training, live online training, and upcoming events, visit the Xilinx Training website, <http://www.xilinx.com/support/education-home.htm>.

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# Documentation

## Context-Sensitive Help

Context-sensitive online Help is available for most ISE Design Suite tools that are available with a graphical user interface (GUI). From Project Navigator, select **Help > Help Topics** to access the online Help or press **F1**.

## Software Manuals

Detailed software manuals about the Xilinx Design Tools and command-line functions are found on xilinx.com. To locate the software manuals on the website:

1. Go to the Documentation Center, <http://www.xilinx.com/support>.
2. Click the **Design Tools** tab.
3. Click the **ISE Design Suite** category and then select version, such as ISE Design Suite 14.7, or click the **See All ISE Design Suite Documentation** link.

## Xilinx Glossary

For a glossary of technical terms used in Xilinx documentation, see:  
<http://www.xilinx.com/company/terms.htm>.

## Licenses and End User License Agreements

The third-party licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx design tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology. You must accept the terms of the End User License Agreements (EULAs) for Xilinx design tools and third-party products before license files can be generated.

To view the third-party license details and EULA, see  
[http://www.xilinx.com/cgi-bin/docs/rdoc?v=14.7;d=ug763\\_tplg.pdf](http://www.xilinx.com/cgi-bin/docs/rdoc?v=14.7;d=ug763_tplg.pdf).

To view the Xilinx design tools license details and EULA, see  
<http://www.xilinx.com/cgi-bin/docs/rdoc?v=14.7;d=end-user-license-agreement.pdf>.

# Older Release Notes

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## ISE Design Suite 14.6

### What's New

#### Device Support

The following devices are production ready:

- Zynq®-7000
  - 7Z010 and 7Z020
- Defense Grade Zynq-7000Q
  - 7Z010, 7Z020 and 7Z030
- Defense-Grade Virtex-7Q
  - VX690T and VX980T
- Defense-Grade Artix-7Q
  - A100T and A200T
- XA Artix®-7
  - A100T

#### Device Support for ChipScope Pro and iMPACT

- 7 Series XQ package & speed grade changes

### Important Information

#### Limited Access Devices

The following devices are Limited Access that require a special license:

**Note:** 7Z100 - Moved from Public Access in ISE 14.5 to Limited Access in ISE 14.6. The 7Z100 will no longer be officially supported by the ISE tools.

- Zynq-7000
  - 7Z100
- Virtex®-7
  - VX1140T, 2000T, H580T and H870T

## Vivado IP Catalog

Readme files included with IP provided through the Vivado IP Catalog and ISE CORE Generator™ tools have been updated to show a running history of new feature additions.

## Updates to Existing IP

- TEMAC
  - Virtex-7, Artix-7, and Zynq-7000 moved to production
- RXAUI
  - Kintex-7, Artix-7, and Zynq-7000 moved to production
- XAUI
  - Kintex-7, Artix-7, and Zynq-7000 moved to production
- QSGMII
  - Kintex-7, Artix-7, and Zynq-7000 moved to production
- 1000BASE-X/SGMII
  - Kintex-7, Artix-7, and Zynq-7000 moved to production
- GMII2RGMII
  - Zynq-7000 moved to production
- PCI32 and PCI64
  - Artix-7 moved to production
- 7 Series Transceiver Wizard
  - Added several new protocol templates
- Aurora 64B/66B
  - V7-GTH characterization updates
  - Hot plug detect support for the Xilinx 7 series FPGAs
  - Validation using KC724 board-to-board



- Clocking Wizard
  - Spread spectrum support added to version 4.2
  - Fast simulation support added to version 4.2
- Distributed Memory Generator v7.2
  - Example test bench support added
    - 10 Gigabit Ethernet MAC
  - Added Artix device support

## System Generator for DSP

- Tools Integration
  - Introducing support for MATLAB® and Simulink® release R2013a on Windows 7 32-bit and 64-bit platforms. To enable support, see [Answer Record 56250](#).

---

# ISE Design Suite 14.5

## What's New

### Device Support

- Support enabled for Zynq™-7000 7Z100 device
- The following devices are production ready
  - Virtex®-7
    - 7VX690T, 7VX330T, 7VX415T, and 7VX980T
  - Zynq-7000
    - 7Z030 and 7Z045
  - Defense-Grade Kintex™-7Q
    - 7K325T and 7K410T
  - Defense-Grade Virtex-7Q
    - 7V585T and 7VS485T

## Important Information

ISE® Design Suite 14.5 has moved from FLEX 11.6 to FLEX 11.11 as the basis for all licensed applications.

## Updates to Existing IP

- PCI EXPRESS® Gen3/Gen2
    - Updated GT wrappers
    - Added Root Port support
  - Added support for Zynq 7030 and 7045 devices
  - 10G Ethernet MAC
    - Kintex-7 production
  - XAUI
    - Kintex-7 production
    - Requires patch to GTH and GTP IP. Refer to Xilinx® Answer Record: <http://www.xilinx.com/support/answers/47684.htm>.
  - RXAUI
    - Kintex-7 production
  - Tri-Mode Ethernet MAC
    - Kintex-7 production
  - 1000BASE-X/SGMII
    - Updated GTP and GTH transceiver files
  - QSGMII
    - New GTP transceiver updates
  - SPI-4.2
    - Virtex-7 production
  - PCI32 and PCI64
    - Kintex-7 production
  - For a detailed list of Xilinx IP Cores, see the [IP Release Notes Guide \(XTP025\)](#)
- 

# ISE Design Suite 14.4

## What's New

### Device Support

- The following devices are Production ready

- Artix™-7 100T and 200T
- Zynq™-7000 Z7020
- Support enabled for XA Spartan®-6 LX45/LX75 device in CSG484 Package
- Zynq-7000 device support added to `write_ibis`

## Partial Reconfiguration

Partial bitstream generation is enabled for Artix-7 devices.

## ChipScope Pro Tool and iMPACT

- Zynq QSPI (Quad Serial Peripheral Interface) Flash programming
  - Includes support for iMPACT and Software Development Kit (SDK) Flash Writer
  - Includes support for single (x4) and dual (2x4's in parallel) modes
  - Includes support for Micron Technology Inc. and Spansion Inc. QSPI Flash
- Zynq NAND Flash programming
  - Includes support for iMPACT and SDK Flash Writer
  - Includes bad block management
  - Includes support for Micron Technology Inc. and Spansion Inc. NAND Flash

## System Generator for DSP

- New model upgrade feature for seamless migration System Generator models to use the latest version of superseded blocks.
- New floating-point blocks: Multiply add, accumulator and exponential.
- A 5x simulation time improvement for DSP48 Macro block. Models using many DSP48 Macro blocks see a significant simulation-time improvement.

## Device Support

Virtex-7 Low Voltage (0.9V) devices are no longer supported.

## Updates to Existing Intellectual Property

- SGMII over LVDS (Synchronous)
  - Added Artix device support
  - Added Zynq device support
- Tri-Mode Ethernet MAC

- Added support for the AC701 board for the core example design
  - Soft Error Mitigation
    - Pre-production support for an updated Spartan-6 Readback Solution
    - Pre-production support for Virtex-7 SSI, Artix-7 devices, and Zynq devices
  - IBERT 7 series GTZ support for Virtex-7 FPGA devices
    - IP CORE generation for line rate up to 28.05 Gb/s
    - Logic analyzer support for RX Margin Analysis, including 2D Eye Scan measurement
  - 7 Series Transceiver Wizard
    - Added several new protocol templates
  - Aurora 8B/10B
    - Virtex-7 GTH device hardware validation
    - Artix-7 GTP device hardware validation
  - Aurora 64B/66B
    - Virtex-7 GTH device hardware validation
    - Virtex-7 HT, GTZ device support
  - PCI EXPRESS® Gen3/Gen2
    - Tandem PROM/PCIe® configuration support (Beta)
    - Gen2 IP in production for production devices
  - For a detailed list of Xilinx® IP Cores, see the [IP Release Notes Guide \(XTP025\)](#)
- 

## ISE Design Suite 14.3

### What's New

#### Device Support

- The following devices will be Production ready
  - Kintex™-7 70T, 480T, 420T, 355T, 325T (Low Voltage), 160T (Low Voltage), 410T
  - Virtex-7 X485T (Low Voltage)
- The Virtex-7 X690T device will be General Engineering Sample (ES) ready
- Serial Peripheral Interface (SPI)

- Virtex-6 and Spartan®-6 FPGAs - Core programming time improved by ~2.5x compared to 14.1
- Byte-wide Peripheral Interface (BPI)
  - Xilinx 7 series FPGAs - Core programming time improved by ~3x compared to 14.2

### Partial Reconfiguration

- Partial bitstream generation is enabled for Zynq devices.
- Global Set Reset (GSR) introduced for partial bitstreams (Virtex-6 & 7 series) - partial reconfiguration regions can utilize the dedicated global set / reset capabilities to initialize elements after reconfiguration by tagging Reconfigurable Partitions with the RESET\_AFTER\_RECONFIG attribute.

### iMPACT

- Indirect programming of NOR Flash through PS for Zynq devices
- Indirect erase, program, and readback/verify of NOR Flash through PS

### Error Correction Code IP

- New Error Correction Codes (ECC) IP – Pre-production
  - ECC Encoder
  - ECC Decoder
  - ECC Encoder/Decoder – Combine both encoder and decoder operations in a single module
  - ECC Clock Enable and registering options

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## ISE Design Suite 14.2

### What's New

#### Device Support

- Production support for the following devices:
  - Kintex-7 325T
  - Kintex-7 410T
  - Virtex®-7 X485T

- Performance increase of ~3.5% for the -2 speed grades for Kintex-7 and Virtex-7 FPGAs
- Artix-7 FPGA family now supports bitstream generation
- Partial Reconfiguration support added for Zynq-7000 EPP devices

## Partial Reconfiguration

- Per-frame CRC checks can be done on partial bitstreams (7 series)

## PlanAhead Design Tool

- Clock Planner Fly Lines - the clock tree view for physical device resources now displays fly lines to help the user visualize physical connectivity in the device.

## Pin Planner

- Export menu item from I/O ports view
- Improved handling of diff pairs creation
- Support buses with ascending, descending, and negative bit indexes
- Expand selection menu item in I/O ports view
- Improved rendering focus on a cell in tables and trees
- Improved various views such as SSN report, I/O port property editing, port rendering in package view, and clock resources view
- Improved DRC for VCCAUXIO, VCCAUXIOBT, VCCAUXIOSTD

## System Generator for DSP

- MATLAB® 2012a support
- Blockset Enhancements
  - Floating Point Natural Log
  - Floating/Fixed Point Abs
  - Interleaver/De-interleaver 7.1
- Demos and Examples Updated to target Kintex-7 device

## IP Core Details

### GMII to RGMII

- Connects seamlessly to Zynq Gigabit Ethernet Controller

### SMPTE SDI

- Support SD/HD/3G-SDI uncompressed serial digital video streams in the Xilinx 7 series FPGAs
- Verilog support only

### Core Update Details

For detailed information on core updates in 14.2, see [IP Core Generator Technology](#).

## Important Information About This Release

### Device Support

- Designs targeting the following devices must be re-implemented (place and route) in this release of the software:
  - All Artix-7 devices
  - Zynq™-7000 EPP 7z030 and 7z045 devices
- Xilinx recommends all customers re-run implementation through timing analysis for all designs before generating bitstream in this version of the software.
- Support for the following General ES -2 speed grade devices require patches with this software release (see Xilinx Answer Record 50886 at <http://www.xilinx.com/support/answers/50886.htm>).
  - Kintex-7 325T, 480T, 420T and 410T
  - Virtex-7 X485T and 2000T

### Memory Interface Generator

All customers must re-generate their memory controller design with MIG 7 Series Version 1.6.

### Invoking Xilinx Tools from the Command Line in Linux OS

For commands to invoke Xilinx tools in Linux OS, see Xilinx Answer Record 41265 at <http://www.xilinx.com/support/answers/41265.htm>.

### IP Core Generator Technology

#### Updates to Existing IP

- 7 Series Transceiver Wizard
  - Added several new protocol templates

- Added Zynq 7045 (GTX) device support
- Aurora 64B/66B
  - V7-GTH characterization updates
  - Hot plug detect support for the Xilinx 7 series FPGAs
  - Validation using KC724 board-to-board
- Aurora 8B/10B
  - Virtex-7 GTH device support
    - Super Logic Region (SLR) support
  - 16-bit additive scrambler/descrambler
  - 16-bit or 32-bit CRC for user data
  - Hot-plug detect support for the Xilinx 7 series FPGAs
  - Updated test bench
  - Validation using KC724 board-to-board
- ChipScope™ Pro IP Core
  - IBERT 7 Series GTH support for Virtex-7 FPGA devices
    - Analyzer support for RX Margin Analysis, including 2D Eye Scan measurement
  - IBERT 7 Series GTP support for Artix-7 FPGA devices
    - CORE Generator™ tool support
    - Analyzer support for basic measurements
  - IBERT 7 Series GTZ support for Virtex-7 FPGA devices (Limited Access via Virtex-7 HT GTZ lounge only)
    - Analyzer support for basic measurements
- Clocking Wizard
  - Spread spectrum support added to version 3.6
- Distributed Memory Generator v7.2
  - Example test bench support added
- PCI EXPRESS Gen3/Gen2
  - IP support
  - Beta features for Tandem PROM/PCIe
- 10 Gigabit Ethernet MAC
  - Added Artix device support



- Added Zynq device support
- 1000BASE-X/SGMII
  - Added Artix device support
  - Added Zynq device support
  - Added SGMII over LVDS sync support for Virtex-7 and Kintex-7 families
- AXI Ethernet
  - Added Zynq device support

#### **Additional IP Supporting AXI4 Interfaces**

- The latest versions of CORE Generator IP have been updated with Production AXI4 interface support. For more detailed AXI IP support information see [http://www.xilinx.com/ipcenter/axi4\\_ip.htm](http://www.xilinx.com/ipcenter/axi4_ip.htm).
- In general, the AXI4 interface is supported by the latest version of an IP, for Zynq-7000 EPP and Virtex-7, Kintex-7, Virtex-6 and Spartan-6 devices families. Older “Production” versions of IP continue to support the legacy interface for the respective core on Virtex-6, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 devices families only.
- For general information on AXI4 support, see <http://www.xilinx.com/ipcenter/axi4.htm>.
- A comprehensive listing of cores that have been updated in the 2012.2 release can be viewed at [www.xilinx.com/ipcenter/coregen/updates\\_14\\_2\\_2012\\_2.htm](http://www.xilinx.com/ipcenter/coregen/updates_14_2_2012_2.htm).

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## **ISE Design Suite 14.1**

### **What's New**

#### **Device Support**

- Public access is now available for the following families:
  - Zynq™-7000 EPP (including bitstream generation)
  - Defense-grade 7 series FPGA and Zynq-7000 EPP
  - Automotive XA Zynq-7000 EPP
- Virtex®-7 XT FPGA family now supports bitstream generation.
- Artix™-7 FPGA GTPE2 support is now available, which includes:
  - SecureIP simulation models for all Xilinx-supported simulators.
  - 7 series FPGA GT Transceiver Wizard support.

- The following Artix-7 devices have been removed from the tools:
  - XC7A8
  - XC7A15
  - XC7A30T
  - XC7A50T
- ISE® Design Suite requires users to select all I/O Standards and pin-placement in their designs prior to generating a bitstream. See the following Xilinx Answer Record for more information: <http://www.xilinx.com/support/answers/41615.htm>

## PlanAhead Design Tool

More information on new features described in this chapter can be found in the *PlanAhead Design Tool User Guide*:

[www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_1/PlanAhead\\_UserGuide.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_UserGuide.pdf)

### General

- The Flow Navigator now provides a more detailed view of the steps involved in the compilation flow. This includes the ability to collapse and expand the list of detailed tasks available within each design view (RTL Analysis, Synthesis, Implementation, and Program and Debug).
- The new clock resource view now displays connectivity of clocking and I/O related resources using fly lines.
- Project settings now include more XPA options.

### Pin Planning

- The PlanAhead™ design tool now provides the ability to convert pin-planning projects from an empty netlist project to a full RTL or netlist-based project. This allows you to migrate pin planning projects to more useful projects that manage more source types.
- Pin-planning support for Zynq-7000 EPP devices is now available.
- Pin-planning projects can now automatically infer differential pairs by recognizing one side of a differential standard and by providing the ability to automatically create the other side of the differential pair.
- There is an improved Simultaneous Switching Noise (SSN) reporting engine and improved 7 series FPGA noise prediction.
- There are improvements on the presentation of default I/O standards.

### Modelsim & Questa Advanced Simulator Integration

- The PlanAhead design tool now allows you to choose Modelsim or Questa® Advanced Simulator as the target simulator in the project settings. Simulation requires library

compilation, which can be accomplished through Tcl command `compplib`. The main advantage of this integration over ISE tools integration is the ability to have multiple simulation filesets with their own sets of properties. This allows you to simultaneously create and maintain multiple simulation configurations that could vary depending on the testbench being used or other simulation properties.

### Embedded Development Kit Integration

- The PlanAhead design tool can now create and add Xilinx Platform Studio (XPS) subsystems to a project through the `.xmp` source type. Double-clicking the `.xmp` source type launches Xilinx Platform Studio to generate and customize the embedded subsystem.
- Integration support also includes importing and converting ISE tools projects (`.xise`) that have `.xmp` sources embedded within them to PlanAhead design tool projects. The PlanAhead design tool manages generated files from XPS appropriately in the synthesis and implementation tool flows.

### System Generator for DSP Integration

- PlanAhead design tool can now create and add DSP subsystems to a project through the `.sgp` source type. Double clicking the `.sgp` source type launches The MathWorks Simulink® to generate and customize the DSP subsystem.
- Integration support includes importing and converting ISE tools projects (`.xise`) that have `.sgp` sources embedded within them to PlanAhead design tool projects. PlanAhead design tool manages generated files from the DSP tools appropriately in the synthesis and implementation tool flows.

### IP Repository

- PlanAhead design tool now allows the use of the IP repository without creating a design. You can create an empty project and open the IP repository for browsing, generating, and configuring an IP core. Generated sources, such as example designs, constraint files, data sheets, and more are now viewable in the project with a special IP Sources tab in the sources view.
- Initial support for the IEEE P1735 encryption standards.

### Runs Infrastructure

- PlanAhead design tool can now force a run up-to-date if it has been marked stale and the user wishes to override the tool.
- Physical constraint updates do not cause the synthesis run state to go stale.
- There is a new "next step" option to run to intermediate states of the ISE tools (e.g. `ngdbuild`, `map`, `par`, `trce`).
- Bitgen options are now integrated with run options in project settings.

- There is now support for optional steps in the flow, as well as a mechanism to invoke Tcl “hook” scripts for use between stages of the run flow. You can specify a Tcl script that runs between compilation stages, you can use it for custom workarounds or reporting purposes.

### Project Infrastructure

- Messages are now centralized to a common message manager, and should be visible in the messages tabs.
- PlanAhead design tool can now reset parameters and properties with the new Tcl commands `reset_param` and `reset_property`. These commands reset the value of the property and parameter to the built-in default, and if appropriate, to the specific target device.
- Certain invalid UCF messages are disabled for RTL elaboration.
- Improved falsely reported error and critical warning conditions when parsing UCF on RTL netlists.
- Improved include file support in RTL.

### Embedded Design Tools

Embedded Design improvements in 14.1 are focused on 4 main areas:

- Zynq-7000 EPP support for bare-metal and Linux-based product development
- MicroBlaze™ processor updates
  - Performance improvements
  - New instructions for endianness conversion
  - Pre-integrated I/O module
  - Multi-processor lock-step/result-voting for tamper & single event upset detection
  - Additional device support
- IP updates for improved system performance, configuration, and utility
- Tools updates for XPS and SDK

### Zynq-7000 EPP Support

- 14.1 ISE WebPACK™ design tools now support Zynq-7000 EPP for the Xilinx Z7010, Z7020, Z7030 parts. Included in WebPACK design tools are the same tools as the Embedded Edition – XPS, SDK, MicroBlaze processor, and the full embedded IP library.
- XPS includes new configuration and MIO summary windows dedicated to Zynq-7000 EPP (see Embedded Tools below for further information).

- Zynq-7000 EPP documents are now available on the Xilinx website and also through the Xilinx Documentation Navigator tool which can be downloaded from <http://www.xilinx.com/support>.

### MicroBlaze Processor Updates

- New Low-latency interrupt mode
  - The controller directly supplies the interrupt vector resulting in a reduction in latency response by as much as 10X depending on system design.
- New Swap instructions
  - New instructions for byte and halfword swapping help support endianness conversions between AXI big-endian and AXI little-endian.
- Additional Device Support
  - MicroBlaze processor has been validated across Xilinx 7 series FPGA families.
- System Cache
  - Embedded Edition adds a new embedded system cache IP peripheral between a MicroBlaze processor and external memory controller for AXI-based systems. MicroBlaze processor uses this System Cache IP core as Level 2 cache resulting in lower latency and faster performance depending on multiple system factors, design type, or connection points.
- I/O Module
  - A new, configurable collection of general embedded processor peripherals packaged into a single IP block for connection to the MicroBlaze processor data-side LMB bus. This simplifies the definition, configuration and deployment of a standard Microcontroller system and enables MicroBlaze processor MCS designs to be moved seamlessly from Logic Edition into Embedded Edition.

### Embedded IP Updates

14.1 includes IP core enhancements and additions focus on improved support for AXI, Zynq-7000 EPP, and MicroBlaze processor.

- AXI Quad SPI - Supports Execute In Place (XIP) mode and architectural improvements for performance. This IP core continues to work in Legacy mode as default option for existing customer.
- AXI Performance Monitor - Measures bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, the amount of memory traffic for specific durations, and other performance metrics.
- Processing System7 - Wrapper IP for Zynq-7000 EPP, logic connection between PS and PL to assist with adding custom or other EDK IP.

- AXI System Cache - Level 2 Cache module for MicroBlaze processor when used in between MicroBlaze processor and external memory controller.
- Embedded IO Module - Common I/O peripheral sub-set, introduced in MicroBlaze processor MCS, ported to Embedded Edition for compatibility.

### Embedded Tools

In ISE Design Suite 14.1, the PlanAhead design tool now supports embedded design capture and management and is the recommended embedded design flow.

- What's New in XPS?
  - In 14.1, XPS has been extended to provide Zynq-7000 EPP specific tools for configuration and first-stage bootloader generation with SDK.
    - The new Zynq-7000 EPP Processing System provides developers with dozens of configuration options for memory, clocks, peripherals, DMA, I/O, Interrupts and Flash memory interfaces. XPS now includes a new configuration window which enables users to graphically configure each parameter with guaranteed routing, voltage and clock-correct automated selections.
    - 14.1 includes standard Zynq-7000 EPP configurations (for the ZC702 board), to enable developers to begin work immediately.
    - The new Zynq-7000 EPP MIO summary window provides an aligned, color-coded graphic view of peripheral pin outs for faster, easier and guaranteed-correct MIO selection.
- What's New in SDK?
  - 14.1 now provides Xilinx SDK free of charge with all FlexLM license checks removed. SDK can be installed from a stand-alone installer (available on the Xilinx website) or within each ISE design tools edition installation.
  - Full support for Zynq-7000 EPP
    - SDK now provides a full tools solution for bare-metal and Linux application development and profiling. Such tools include ARM GCC updated for bare-metal (EABI) and Linux development, Boot Image Creator, Flash programmer for QSPI, Device tree generator, and the remote system explorer (debug an IP-connected target board).
    - SDK works with XPS to build and generate design-specific firmware including the first stage boot loader with provision for device security, fallback boot, and bitstream management. It will also combine, build and deploy a complete bootable system image to the Zynq-7000 EPP target platform.

### ChipScope Pro Tool and iMPACT

- Zynq-7000 EPP

- Indirect Quad-SPI Flash programming support through iMPACT
- ChipScope Pro tool device programming and debug support
- iMPACT basic and advanced programming support
- Virtex-7 FPGA
  - IBERT 2-D Eye Scan enhancements
  - 7 series FPGA GTH support
  - ChipScope Pro tool device programming and debug support
  - iMPACT basic and advanced programming support
- Kintex-7 FPGA
  - IBERT 2-D Eye Scan enhancements
  - ChipScope Pro tool device programming and debug support
  - iMPACT basic and advanced programming support
- Artix-7 FPGA
  - Core generator tool and inserter support
- ChipScope Pro tool AXI Monitor now supports EDK and standard CORE Generator tool flows

## System Generator for DSP

- Device support updated to include Defense-Grade 7 Series FPGA and Automotive XA Zynq-7000 EPP families
- PlanAhead design tool integration
  - Integrate System Generator modules in a larger RTL design
  - Includes tutorial
- New “Performance Tips” toolbar button which opens “High Performance Designs” documentation
- Blockset enhanced with FIFO support for embedded register in BRAM configuration

## IBIS Simulation

- 7 series FPGA IBIS support is provided only through the PlanAhead design tool `write_ibis` command
  - IBISWriter is not available for 7 series FPGA Families

## Partial Reconfiguration

- Device support updated to include the XC7VX980T, XC7A200T, and XC7A350T.
  - Bitstream generation for Artix-7 devices is disabled in 14.1
- The list of resources that must remain static-only has been updated to include I/O and configuration components.

## Intellectual Property (IP)

### Device Support

- Pre-production support has been added for the following families:
  - Defense-Grade Virtex-7Q FPGA
  - Defense-Grade Kintex-7Q FPGA
  - Defense-Grade Artix-7Q FPGA
  - XA Artix-7 FPGA
  - XA Zynq-7000 EPP

### New IP Cores

- SMPTE 2022 5/6 Video over IP v1.0 - provides Transmitter and Receiver cores for broadcast applications that require bridging between Broadcast Connectivity standards (SD/HD/3G) and 10G networks.
- Ten Gigabit Ethernet 10GBASE-KR – 10G Ethernet PCS/PMA with optional Forward Error Correction (FEC) and Auto-Negotiation (AN) for 7 series FPGA GTX and GTH transceivers. Delivered as an optional, separately licensed configuration of the Ten Gigabit Ethernet PCS/PMA (10GBASE-R/KR) IP core.
- Asynchronous Sample Rate Converter for Digital Audio - converts stereo audio from one sample frequency to another. The input and output sample frequencies can be either an arbitrary fraction of each another, or the same frequency, but based on different clocks.
- Video In to AXI4-Stream - converts common parallel clocked video signals to an AXI4-Stream interface. This enables connection of external video sources such as a DVI PHY to other video processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP).
- AXI4-Stream to Video Out - converts AXI4-Stream interface signals to a standard parallel video output interface with timing signals. This enables connection of video processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP) to external video sinks such as DVI PHY.
- AXI4-Stream Interconnect - a key interconnect infrastructure IP that simplifies the process of connecting heterogenous master/slave AMBA® AXI4-Stream protocol



compliant endpoint IP. The core routes connections from one or more AXI4-Stream master channels to one or more AXI4-Stream slave channels.

- AXI Performance Monitor - measures major performance metrics for the AMBA Advanced eXtensible Interface (AXI) system. Metrics supported include bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, and the amount of memory traffic during specific periods of time.

### **Virtex-7 FPGA GTH Transceiver Support**

- Pre-production Virtex-7 FPGA GTH support has been added to these IP Cores:
  - Ten Gigabit Ethernet 10GBASE-KR
  - 10GBASE-R
  - RXAUI
  - XAUI
  - QSGMII
  - 1000BASE-X/SGMII

## **Important Information About This Release**

### **Updates to existing IP versions**

- FIFO Generator v9.1
  - Maximum data width increased to 4096 for AXI FIFO configurations
- 7 Series FPGA Transceiver Wizard (GT Wizard) v2.1
  - New example design module for GTX and GTH transceivers demonstrates the initialization sequence described in UG769.
  - Port and Attribute settings updated to support Initial ES (IES) GTH devices
  - New GTX Protocol templates (simulation only): HD-SDI, 3G-SDI, 6G-SDI and PCI Express Gen1, Gen2
  - New GTH Protocol templates (simulation only): XAUI, RXAUI, OTL3.4, OC48, Gigabit Ethernet (1000BASE-X PCS/PMA), QSGMII, CPRI™, PCI Express Gen1, Gen2
  - New GTP Protocol templates (simulation only): DisplayPort, CPRI, Gigabit Ethernet (1000BASE-X PCS/PMA), QSGMI, V-by-One, HD-SDI, 3G-SDI, 6G-SDI, RXAUI, XAUI
- DisplayPort v3.1
  - 5.4Gbps Single Stream transport (SST) support for 7 series FPGA devices from Specification version 1.2
  - Luminance-only mode for Gray scale video users

- Parameterized Bits Per Component (BPC) to reduce memory footprint
- Quad pixel-wide video clock interface
- Secondary Audio (2-channel) option (separately licensed)
- AXI Bus Functional Model (AXI BFM) v2.1
  - Added VHDL examples
  - Support for Synopsys VCS® and Aldec Riviera-PRO™ simulation tools

## AXI4 IP & More Information

In general, the AXI4 interface is supported by the latest version of an IP for Zynq-7000 EPP & Virtex-7, Kintex-7, Virtex-6, and Spartan®-6 FPGA device families. Older "production" versions of IP continue to support the legacy interface for the respective core on Virtex-6, Spartan-6, Virtex-5, Virtex-4, and Spartan-3 device families only.

- The latest versions of CORE Generator tool IP have been updated with Production AXI4 interface support. For more details AXI IP support information see [http://www.xilinx.com/ipcenter/axi4\\_ip.htm](http://www.xilinx.com/ipcenter/axi4_ip.htm).
- For general information on AXI4 support, see <http://www.xilinx.com/ipcenter/axi4.htm>.
- For a comprehensive listing of IP cores in the 14.1 release, see [http://www.xilinx.com/ipcenter/coregen/updates\\_14\\_1\\_2012\\_1.htm](http://www.xilinx.com/ipcenter/coregen/updates_14_1_2012_1.htm).
- For more information on IP New Features and Known Issues, see the IP Release Notes Guide (XTP025): [http://www.xilinx.com/support/documentation/ip\\_documentation/xtp025.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf).