Results of the TCDS FMC serial link tests

V1.0

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1. INTRODUCTION

This document summarizes the qualification tests performed on the serial links of three FPGA Mezzanine Cards (FMCs) [1] targeted for the new Trigger, Control & Distribution System (TCDS) [2] of CMS. The EDA-02708-V1 (Fig.1) hosts two sockets for SFP+ optical modules operating at up to 10Gb/s each. The EDA-02707-V1 (Fig.2) hosts eight sockets for SFP optical modules operating at up to 800Mb/s each. The EDA-02727-V1 (Fig.3) hosts four sockets for SFP optical modules operating at up to 800 Mb/s each as well as a socket for a standard network cable with each of its four differential pairs operating as well at up to 800Mb/s.

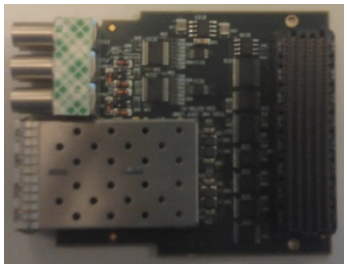

Fig. 1: EDA-02708-V1

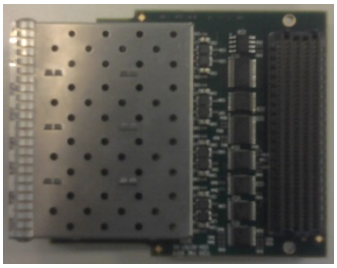

Fig. 2: EDA-02707-V1

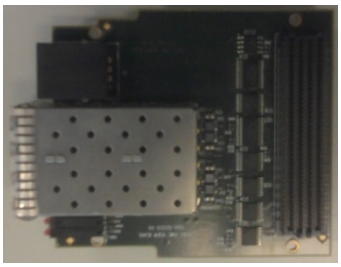

Fig. 3: EDA-02727-V1

The FMC carrier used for the tests is the Xilinx KC705 Evaluation Board [3] shown in (Fig.4). The KC705 among others hosts a Kintex-7 XC7K325T_2FFG900C FPGA, clocking resources and two FMC sockets, one high-pin count (HPC) and one low-pin count (LPC). The KC705 was selected as test platform because the FMC carrier that will be used for the TCDS, namely FC7 [4], is also based on Kintex-7.

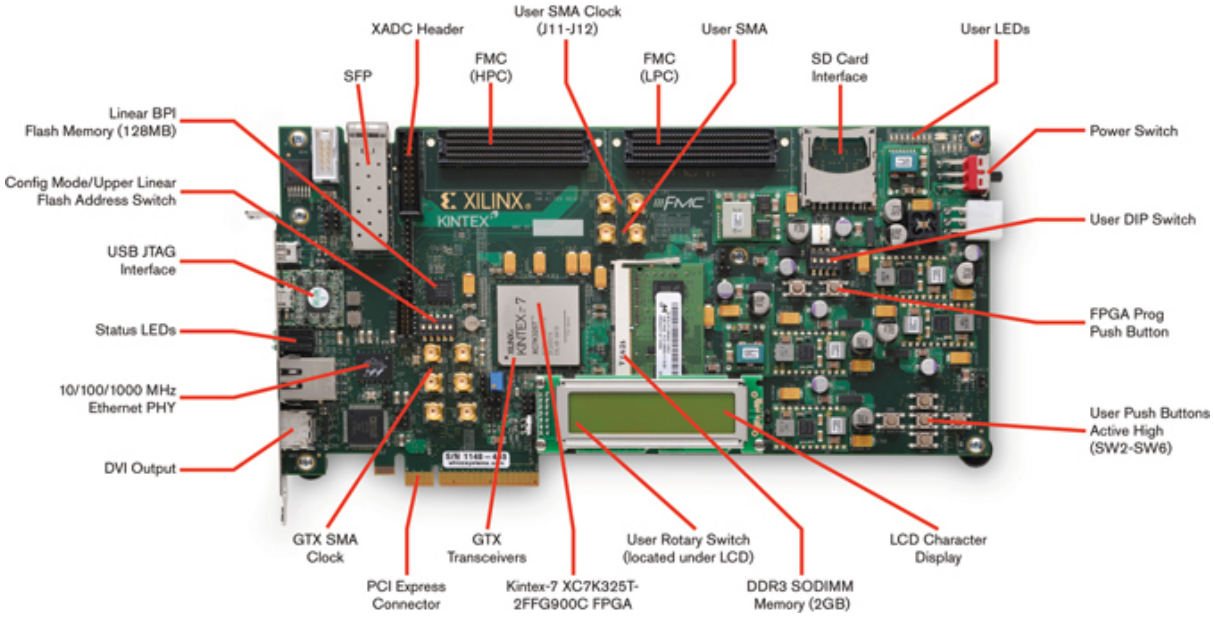

Fig. 4: The KC705 evaluation board

2. TOPOLOGY OF THE TEST

There was a common optical testing topology for all the cards. In addition one more topology is used for LVDS links concerning the card EDA-02727-V1.

2.1. OPTICAL TEST SETUP

A power meter, an attenuator, a splitter, three meters of optical fiber, one SFP and the carrier were used, Figure 5.

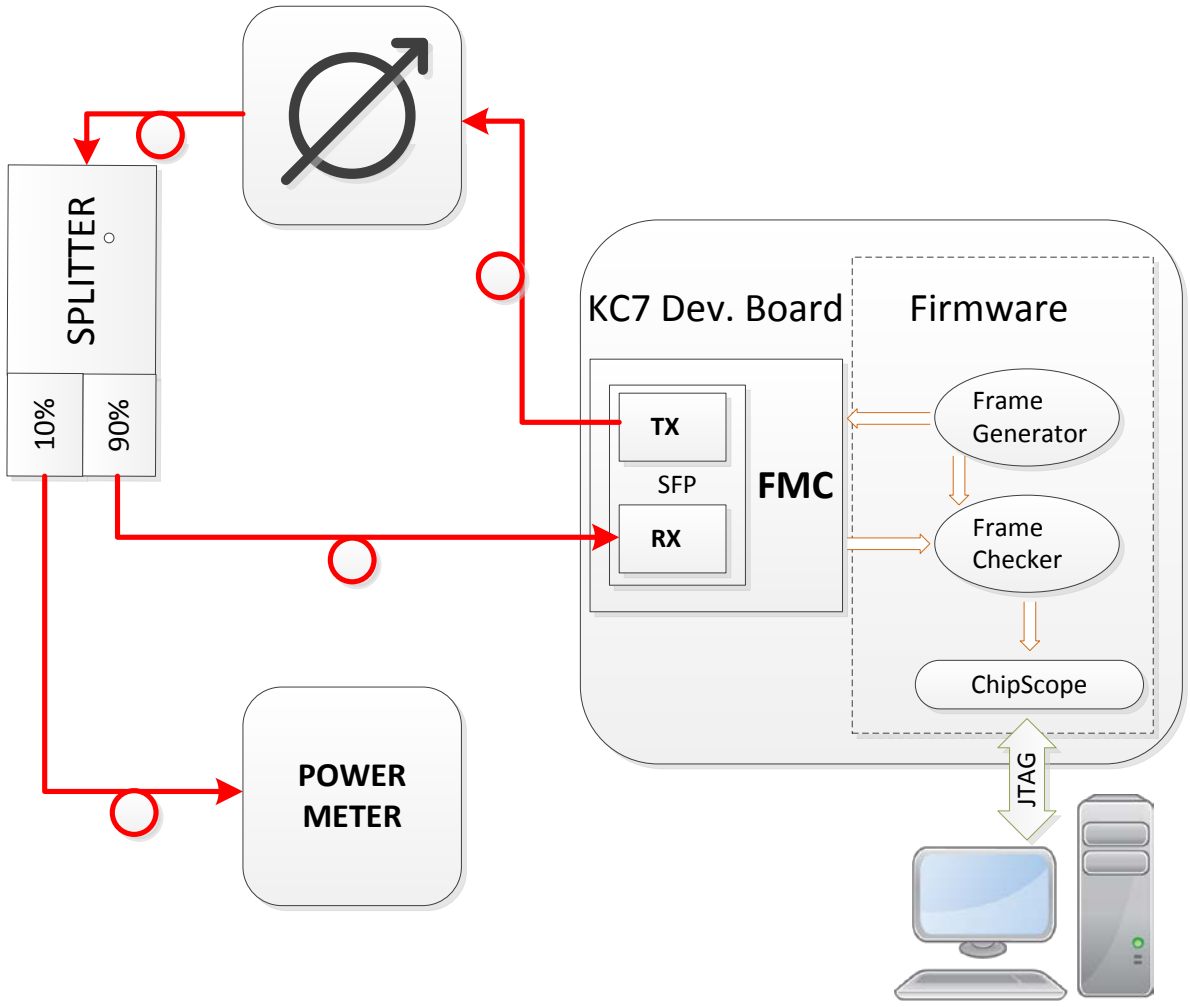

Figure 5: Optical Topology

The logic is designed to generate data patterns, to serialize the data and sent them to the transmitter. The SFP converts electrical signal to optical. Data stream passes through an attenuator. Then the optical signal splits in two and the 90% return to the receiver of the FPGA. The frame checker logic compares the received frame with the delayed frame from the

generator and if they are not equal, the checker increases an error counter. The counter and the frames give to the logic analyser core all the information to have a bit error rate test. The 10% of the splitter goes to a power meter for monitoring. The aim of the test is to meter the BER as the attenuator increases.

2.2. ELECTRICAL TEST SETUP

The figure 6 shows the extra topology used in the third card. In this case there is no way to attenuate the signal. The only way to get the performance of the link is to run the loopback for several hours and note the error free time.

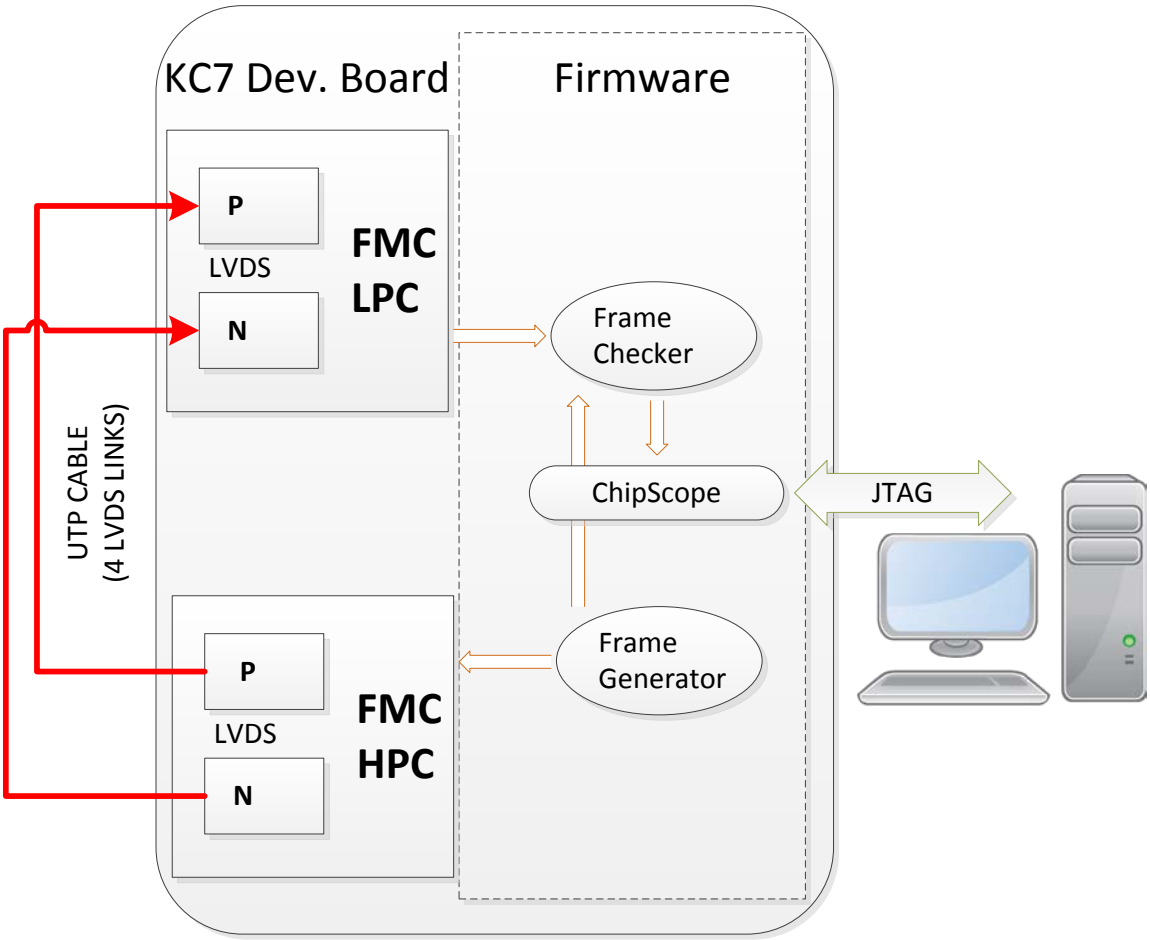

Figure 6: Electrical Topology

There are two EDA-02727-V1 mounted in the carrier. One in the HPC and one in the LPC socket. The Frame Generator sends data to the LVDS link and to the Frame Checker. Two SERDES I/O, are used to loopback data via a UTP cable. Finally the Frame Checker increases the error counter when it finds a mismatch.

3. ARCHTECTURE OF THE FIRMWARE

The firmware designed for the EDA-02708-V1 is the most simple. It contains a Xilinx iBERT core which implements Bit Error Rate logic. In addition I2C VHDL code is implemented to enable the SFPs. The main logic of the firmware for the other two cards is show in the figure7. IOSERDES, 8b10b encoder and decoder frame generator and checkers, MMCMs, state machines counters and an Integrated Logic Analyser (ILA) are used to in order to loopback data. The logic is explained in more detail for each card in the following paragraphs.

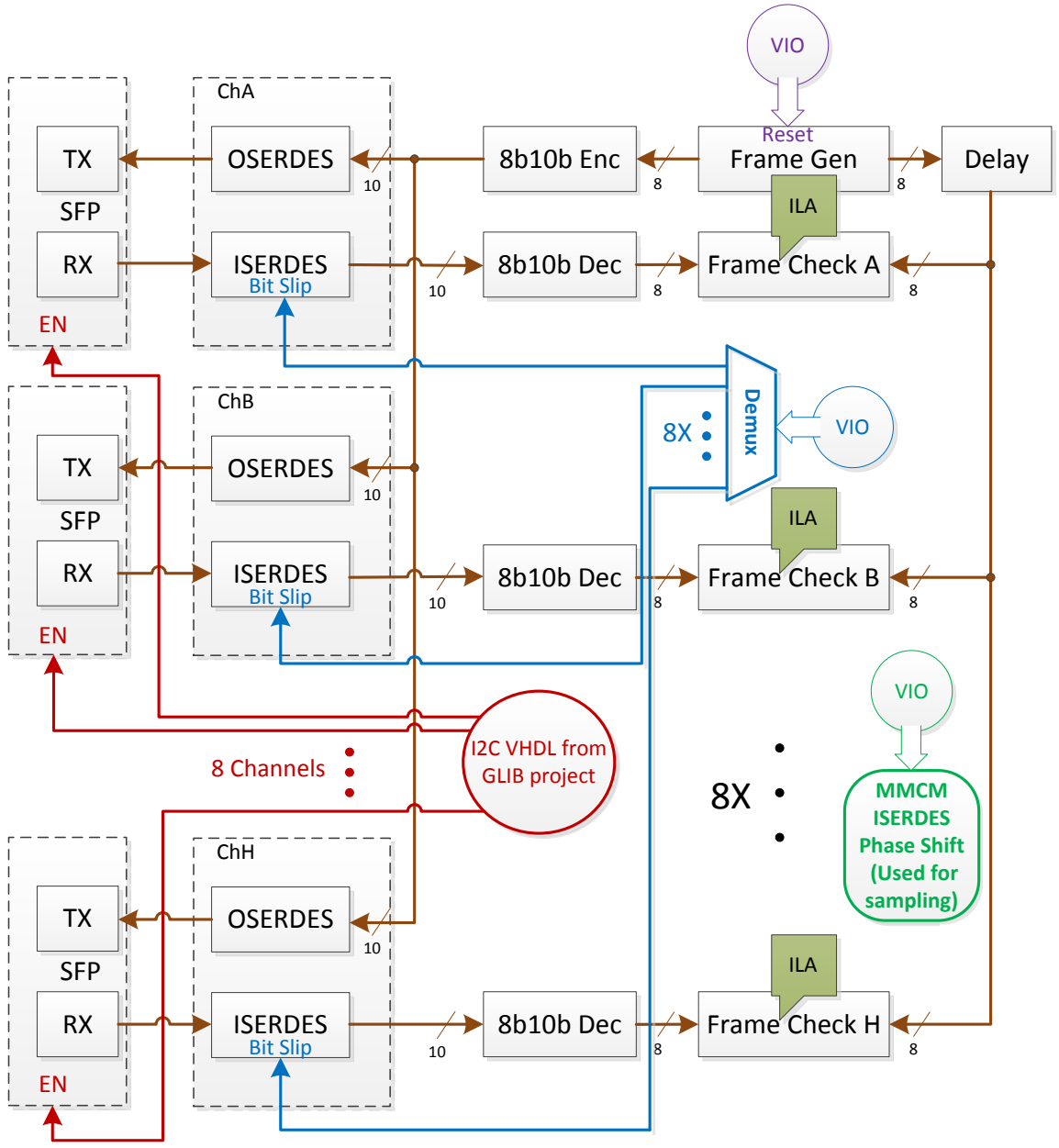

Fig. 7: VHDL code Block Diagram, the main logic

4. MEASUREMENTS

The first test concerns high rate SFP+. In that case GTX transceivers mast be used [5]. The other two has low rate SFP. The GTXs do not support 400Mb/s (starts from 500Mb/s). For low rate SFPs I/OSERDES were used [6].

4.1. TEST OF THE EDA-02708-V1

This card hosts two high rate SFP+ able to run at 10Gb/s [7]. The figure 8 shows the mezzanine mount in the HPC-FMC connector. The architecture uses I2C interface to enable the SFPs, an MMCM (kintex pll), a state machine to control the I2C and an embedded iBERT in order to have the Bit Error Rate test.

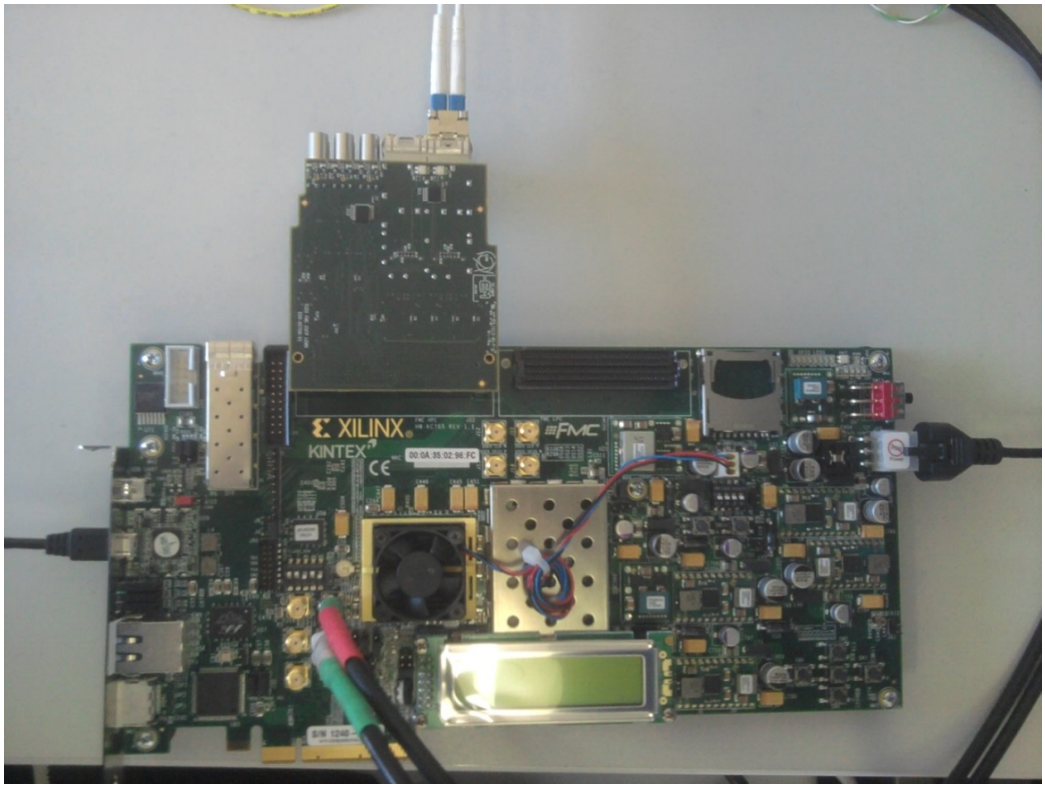

Fig 8: EDA-02708-V1 on the KC705

The test was made in comparison with a commercial card from Faster Technology (S18-B) [8]. The S18-B has 8 channels. The KC705 supports the half of them using the bank 118 of the FPGA. The EDA-02708-V1 on the other hand has two SFPs. In order to compare the two cards the channels X0Y12 and X0Y13 were used. The pattern used for the test was PRBS-7. The results for both cards were very similar (figure 10). The blue curve was from the on board SFP and was the best BER because it has the better PCB path on the KC705 in comparison with the others.

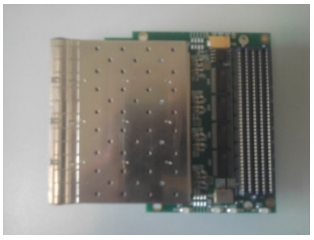

Fig. 9: S18-B

Table 1: Bit Error Rate measurements for the EDA-02908-V1 in comparison with the S18-B

High Pin Count											
EDA-02708-V1						Faster Technology HPC (S18-B)					
X0Y12 (GTX0_118) DP0			X0Y13 (GTX1_118) DP1			X0Y12 (GTX0_118) DP0			X0Y13 (GTX1_118) DP1		
power meter (dBm)	dBm	BER	power meter (dBm)	dBm	BER	power meter (dBm)	dBm	BER	power meter (dBm)	dBm	BER
-31.33	-21.79	3.1E-03	-31.47	-21.93	2.5E-03	-32.23	-22.69	6.6E-03	-32.42	-22.88	7.7E-03
-30.66	-21.12	1.1E-03	-30.65	-21.11	8.1E-04	-31.59	-22.05	2.2E-03	-31.60	-22.06	2.1E-03
-29.95	-20.41	3.5E-04	-29.98	-20.44	2.2E-04	-30.86	-21.32	8.1E-04	-30.58	-21.04	4.4E-04
-29.07	-19.53	5.5E-05	-28.85	-19.31	1.8E-05	-29.45	-19.91	1.0E-04	-29.30	-19.76	4.1E-05
-28.60	-19.06	1.6E-05	-27.74	-18.20	6.2E-07	-28.59	-19.05	1.5E-05	-28.60	-19.06	7.6E-06
-27.88	-18.34	1.4E-06	-26.90	-17.36	5.1E-08	-27.25	-17.71	4.3E-07	-27.41	-17.87	2.4E-07
-27.05	-17.51	3.5E-08	-26.31	-16.77	3.2E-10	-26.38	-16.84	7.5E-09	-26.66	-17.12	9.7E-09
-26.75	-17.21	6.1E-09	-26.01	-16.47	4.1E-10	-25.70	-16.16	1.7E-11	-25.75	-16.21	3.3E-11
-26.46	-16.92	9.8E-10									
-25.97	-16.43	6.7E-11									

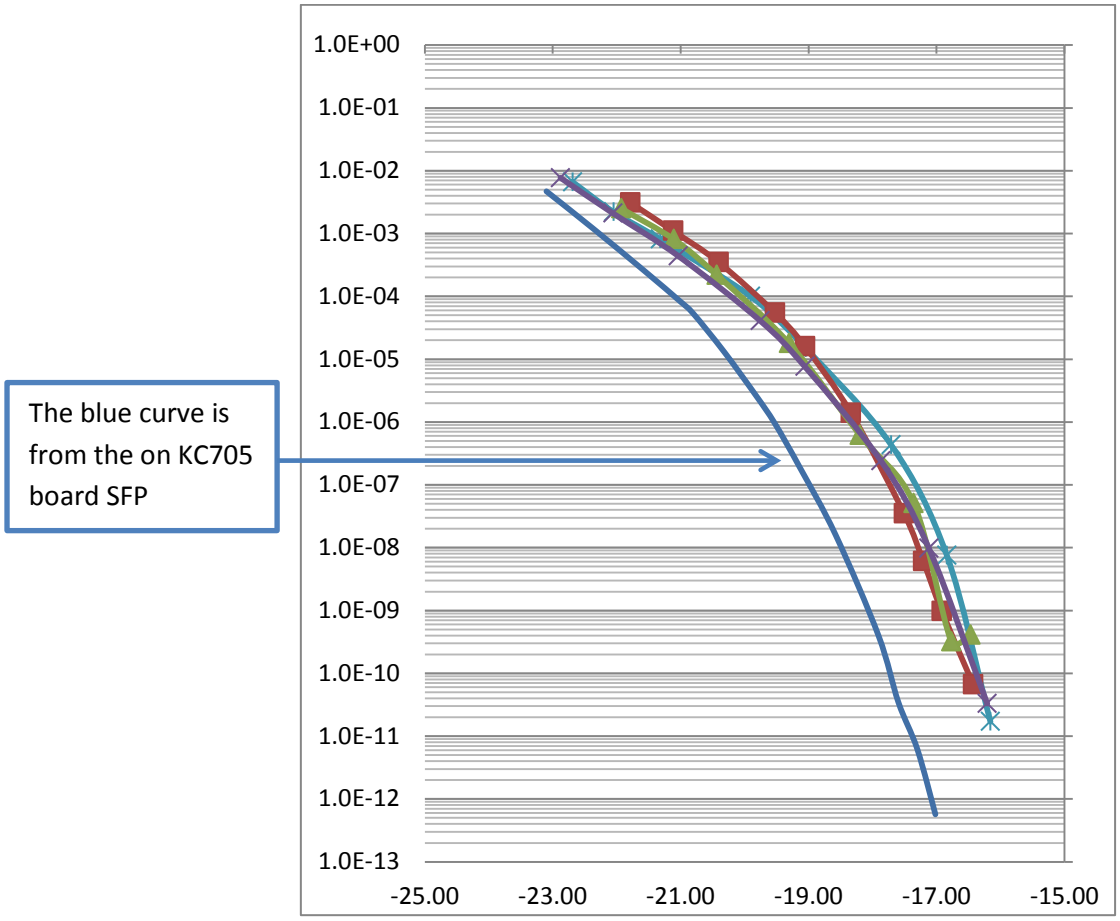

Figure 10 Bit Error Rate curves

4.2. TEST OF THE EDA-02707-V1

This card has eighth low rate SFPs able to run at 400Mb/s [9]. The figure 11 shows the card mounted in the Xilinx board. The firmware implements two MMCMs, one I2C interface to enable the SFPs, one common frame generator (simple counter), one common 8b/10b encoder, eight serializes, eight deserializes, eight 8b/10b decoders, one state machine for bit slip, one synchronous demultiplexer, eight error counters (one for each channel) and two ILA (Indegraded Logic Analyser) cores to illustrate signals (one for the common generator and one for the received frames). The VHDL architecture is shown at figure 10. In order to sample the received data correctly the user can change the phase of the ISERDES clock dynamically using the MMCM phase shift. That has been also implemented.

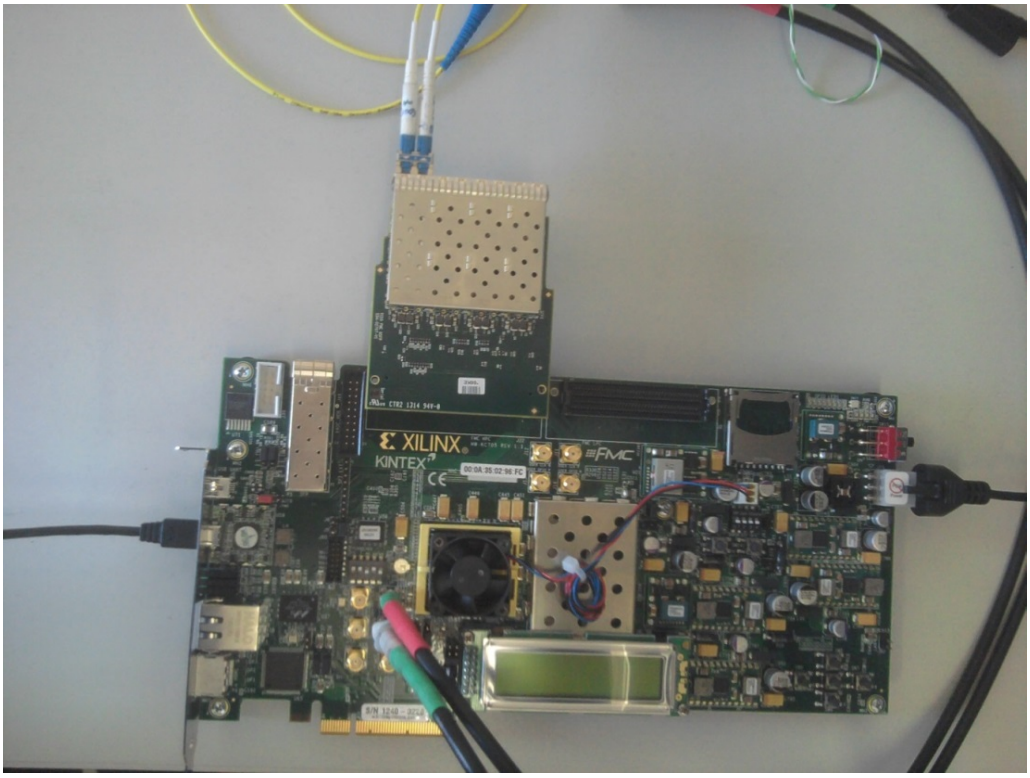

Fig 11: EDA-02707-V1 on the KC705

There were two different bandwidth tests. Fist at 400Mb/s and second at 800Mb/s. In both cases the user increases the attenuator until the channel start to have errors. But before the test the channel has to be calibrated. To do that the frame generator has to send zeros and the user has to shift the phase of the ISERDES several times until the received frame became stable. Then bit slip until only zeros appear. Finally the frame generator starts and then the error counter increases if there is an error. The tables 2 and 3 below show the attenuation

limit. More attenuation than those limits increases the channel error counter. As it can be seeing all the values are very close to –20dBm.

Table 2: Testing at the nominal rate

	CHANNELS at 400Mb/s				
	H	**F**	**D**	**B**	
P.Meter	-29.71	-30.10	-29.97	-30.12	dBm
splitter 10/90%	-20.17	-20.56	-20.43	-20.58	dBm
	G	**E**	**C**	**A**	
P.Meter	-29.06	-29.69	-29.08	-29.66	dBm
splitter 10/90%	-19.52	-20.15	-19.54	-20.12	dBm

Table 3: Testing at double the nominal

	CHANNELS at 800Mb/s				
	H	**F**	**D**	**B**	
P.Meter	-29.09	-30.56	-30.55	-29.96	dBm
splitter 10/90%	-19.55	-21.02	-21.01	-20.42	dBm
	G	**E**	**C**	**A**	
P.Meter	-30.03	-29.21	-30.11	-30.93	dBm
splitter 10/90%	-20.49	-19.67	-20.57	-21.39	dBm

The figures 12 and 13 show the eye diagram of the H channel at both rates.

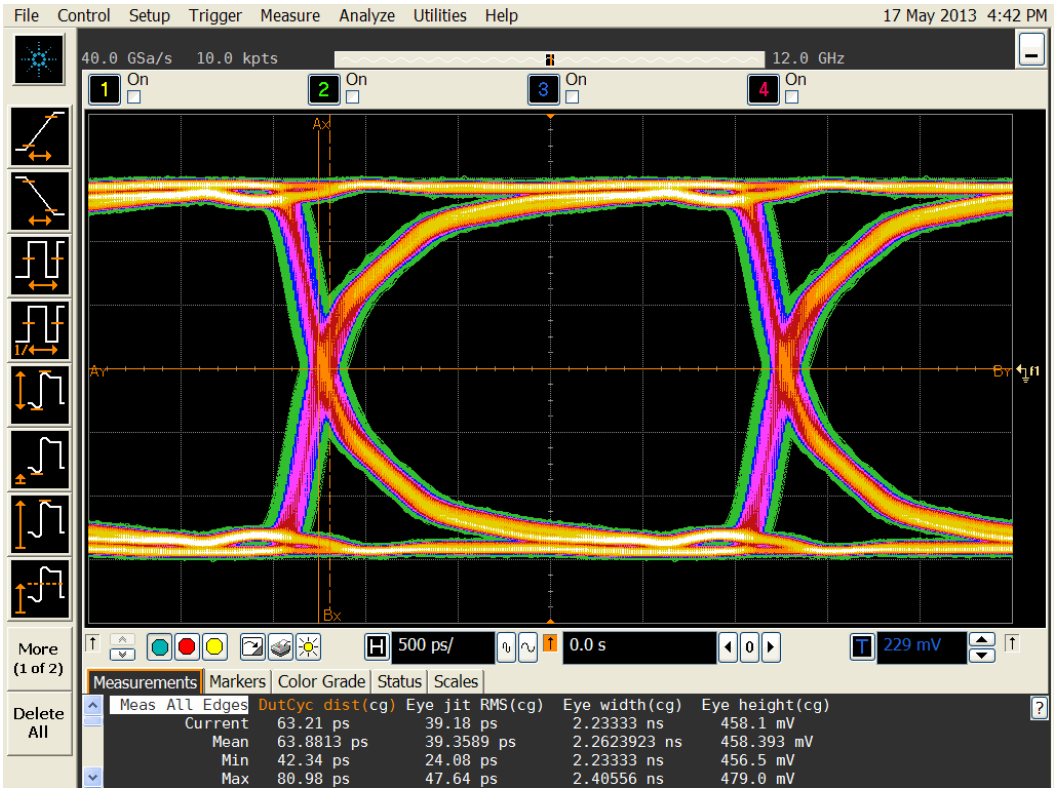

Figure 12: Eye diagram at 400 Mb/s

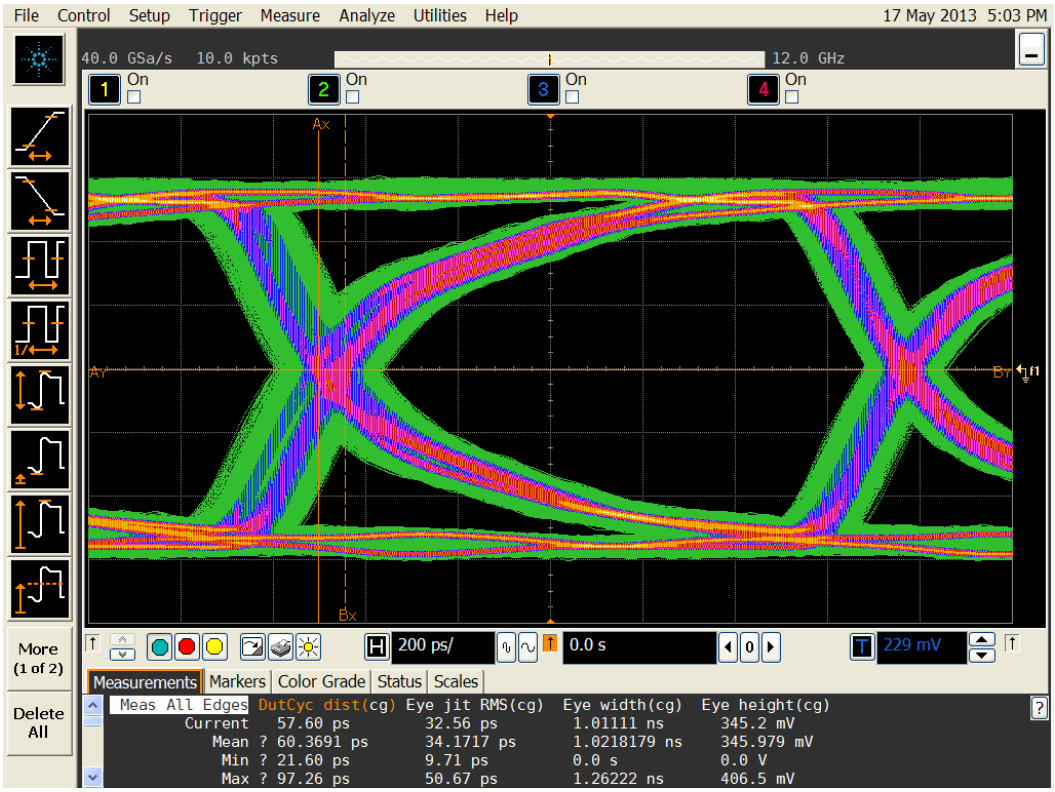

Figure 13: Eye diagram at 800 Mb/s

4.3. TEST OF THE EDA-02727-V1

This card has four low rate SFPs able to run at 400Mb/s [10]. The logic is same as the previous test. The firmware implements two MMCMs, one I2C interface to enable the SFPs, one common frame generator (simple counter), one common 8b/10b encoder, eight serializes, eight deserializes, eight 8b/10b decoders, one state machine for bit slip, one synchronous demultiplexer, eight error counters (one for each channel) and two ila copes to illustrate signals (one for the common generator and one for the received frames). In order to sample the received data correctly the user can change the phase of the MMCM dynamically. The difference with the previous firmware were that in the case of EDA-02727-V1 two carts are used, one in the HPC (High Pin Count) connector and one in the LPC (low Pin Count) connector. The data were not loop backed only by SFPs, but also between HPC and LPC by differential LVDS signals. As it is shown in the figure 13 every card has one RJ45 jack and a UTP cable connects them. Four cable couples loop back the data.

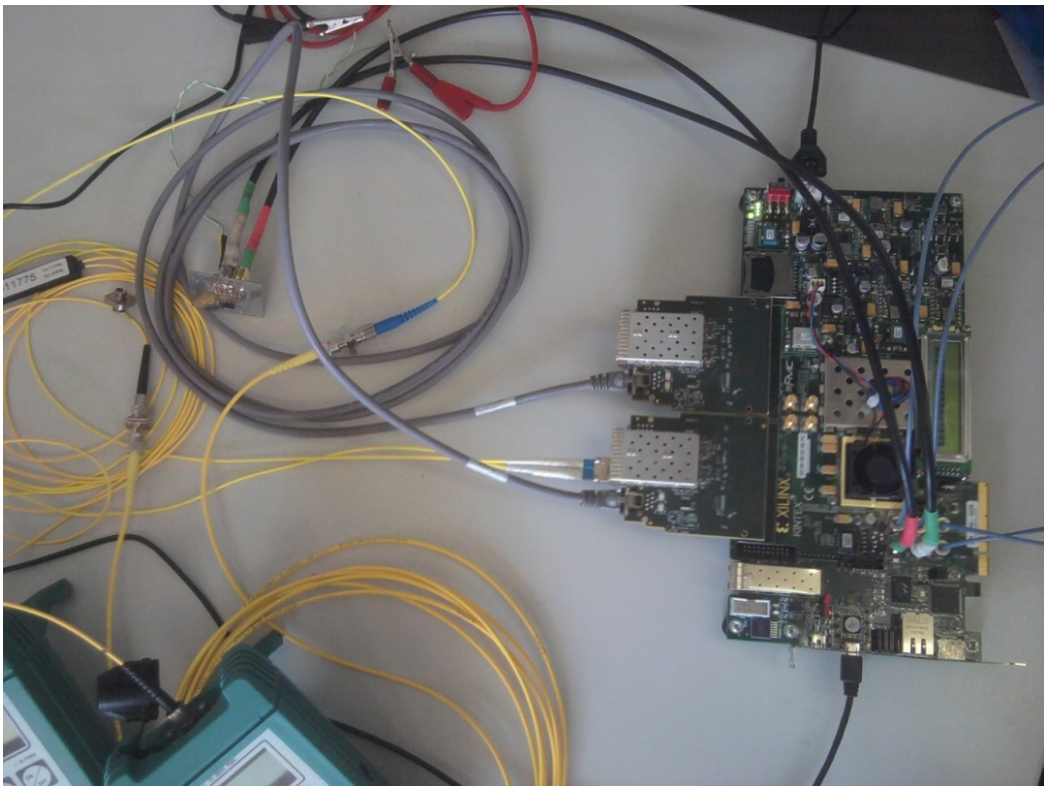

Fig 14: Two EDA-02727-V1 on the KC705

Same as in EDA-02707-V1 there were two different bandwidth tests. The fist at 400Mb/s and second at 800Mb/s. In both cases the user increases the attenuator until the channel start to have errors. Calibration also needed and is the same as mentioned in 4.2 paragraph. The tables 4 and 5 show the attenuation limits. The values are very close to –20dBm. For the channels E, F, G and H the signal cannot be attenuated due to the fact that a copper cable was used. For that link was running for several hours with no error occurred.

Table 4: Testing at the nominal rate

	D	**B**	
P.Meter	-29.95	-30.16	dBm
splitter 10/90%	-20.41	-20.62	dBm
	C	**A**	
P.Meter	-29.88	-30.24	dBm
splitter 10/90%	-20.34	-20.7	dBm

Table 5: Testing at double rate

	D	**B**	
P.Meter	-30.09	-29.71	dBm
splitter 10/90%	-20.55	-20.17	dBm
	C	**A**	
P.Meter	-30.12	-30.46	dBm
splitter 10/90%	-20.58	-20.92	dBm

5. SUMMARY & CONCLUSION

The EDA-02708-V1 in comparison with the commercial mezzanine shows that both cards behave the same at 10Gb/s. When the attenuation was at -16 dBm in the BERT diagram the bit error rate ratio had power of -11. The EDA-02707-V1 and the EDA-02727-V1 run very well at 400Mb/s and also at 800Mb/s. In both bandwidths the attenuated limit was approximately -20dBm. Finally the UTP case as well as in the other tests the system was running for one day without to change the error counter.

REFERENCES

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