A new architecture in multiple lane optical links running at 9.6Gb/s for Drift Tube Track Finder (DTTF) processors in the L1Trigger Upgrade of CMS Experiment at CERN.

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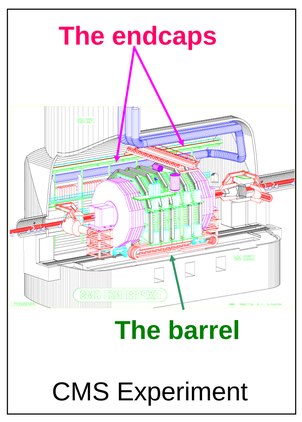
Introduction

Among the other detectors the CMS muon system includes Drift Tubes (DT) to detect muons in the barrel region[1]. The barrel is divided in five wheels. Every wheel has 12 Sectors and each Sector is served by four Minicrates, which are housing the electronics of DTs. The trigger primitives generated in the Minicrates indicate eventual muon passage from the barrel area. The data from the DTs go to the Sector Collector and then to the DTTF (DT Track Finder). Tracking algorithms[2] are implemented to calculate muon parameters for the level 1 trigger. Afterwards data of the muon candidate are forwarded to the next state of the trigger chain, the Global Muon Trigger. New Sector Collectors (TwinMux) are proposed for the level 1 trigger upgrade. Each TwinMux serves two sectors and three DTTF processors. Two optical links at 9.6Gb/s for every sector are used. In addition the TwinMux sends copies of links to DTTF neighbors. The DTTF input will be 30 links serving15 sectors (3 full wedges). Every DTTF processor is scanning for muon track candidates in one wedge and therefore it receives the data from the two neighbor wedges. The processors also exchange data with CSCTFs (Cathod Strip Chamber Track Finders) using additional 9.6Gb/s links. For the moment the old (Altera) algorithms have been implemented in the new Xilinx FPGAs.



Hardware:
Currently at Ioannina a Spartan-6 development board is used with 4 GTPs and at Athens a Virtex-5 with 6 GTPs but very soon both will be equipped with new Virtex-7 and Kintex-7 boards. The current design merges the optical links by configuring GTP Transceivers as follows:

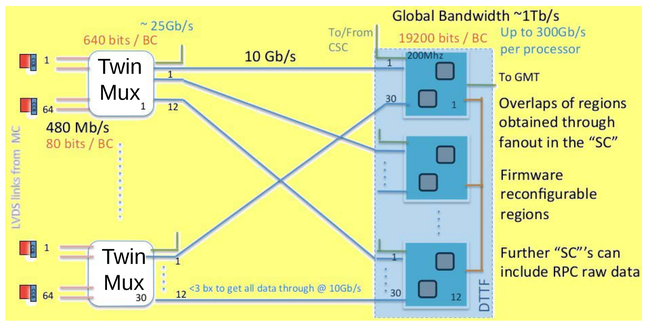
- Aurora multilane 10b/8b Protocol template.
- Lane rate at 3.2Gb/s (Payload at 2.56Gb/s and 32bits@80MHz).
- Data alignment, channel bonding and clock correction.
- External reference clock at 160MHz and PLL usage.

More hardware:
The Greek teem in addition will get:

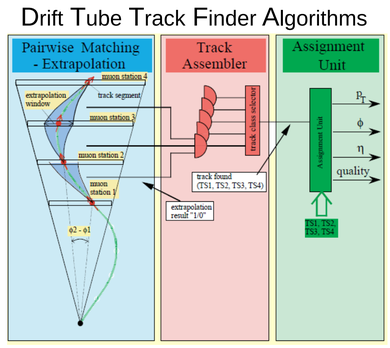
- A μTCA MP7 card (designed by John Jones and Greg Iles in Imperial College). The card is using a mid-range Virtex-7 with GTX or GTH transceivers, up to 72 links at 13.1Gb/s.
- A μTCA crate, each with additional clock and power modules.
- Additional SFP+ and multimode fibers for testing the new development boards.

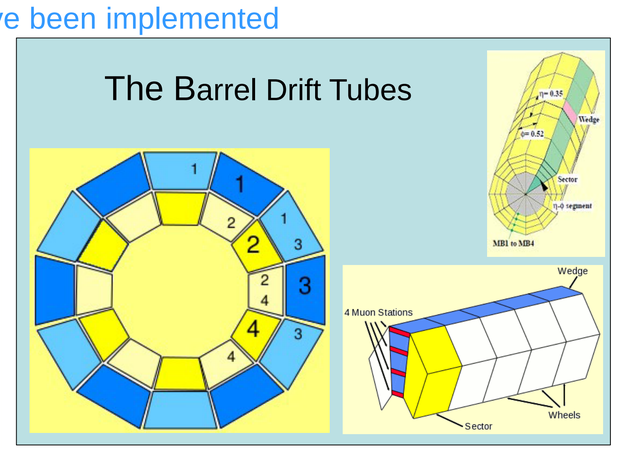
The aim is to develop firmware for the MP7, to control the input and output optical links of the new DTTF processor.

The **Twin Mux – DTTF** Interface



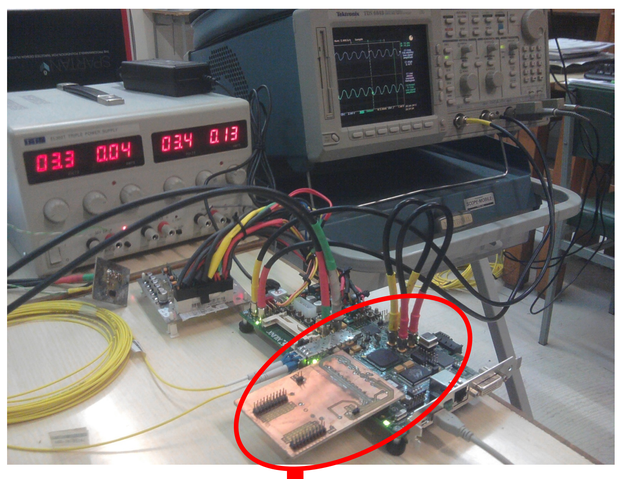
Drift Tube Track Finder Algorithms

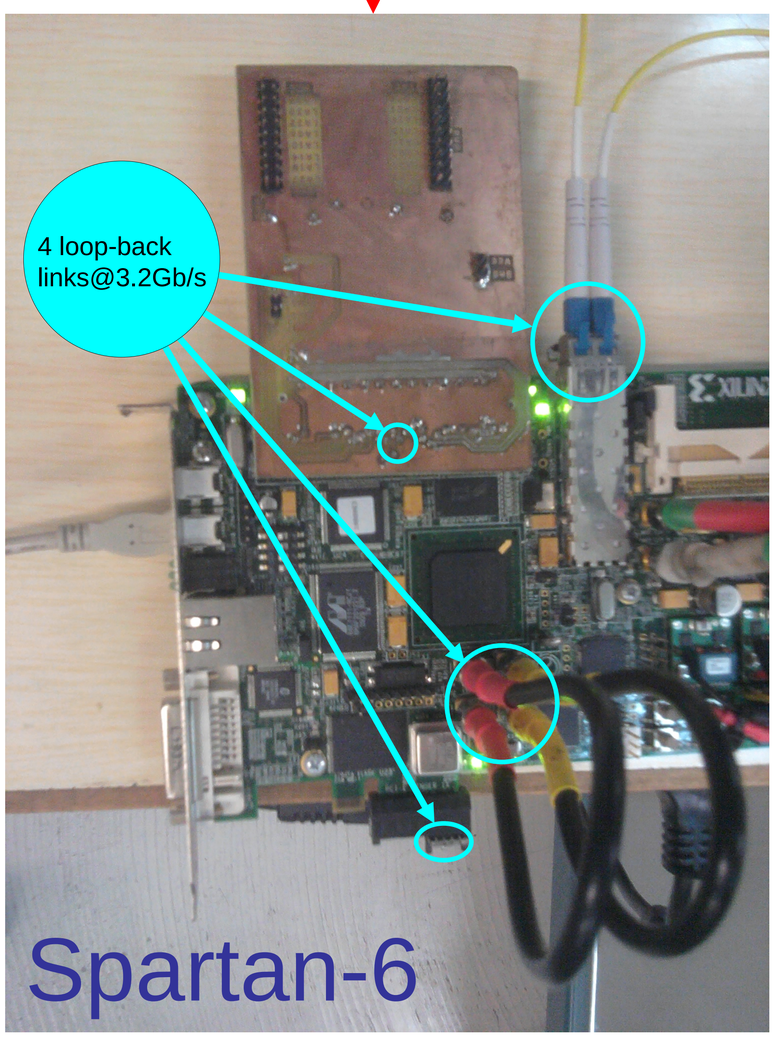




Emulation of the final system

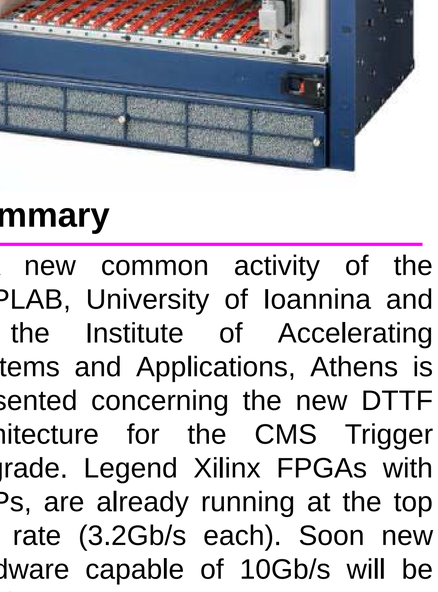
➢ The SP605 board is used for firmware development. The GTP transceiver[3] clock is taken to be synchronous with the LHC clock (40MHz). The four SP605 transceivers run at 3.2Gb/s and after the 10b/8b en/decoding 64bits per bunch crossing are received. The four GTPs stay in phase by channel bonding and the data are aligned by a data alignment procedure (K characters). Finally the links exports 256bits at 25ns, 80% of one Sector's Trigger Primitives. The Virtex-5 has six links and serves more than one full Sector (384bits of 320bits).



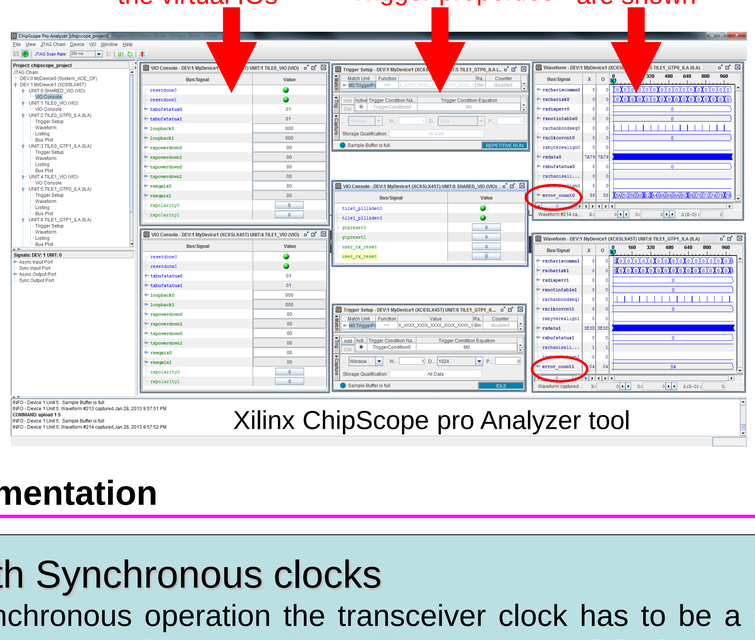


Simulation and Intergraded Logic Analyzer

➢ The design uses a 160MHz external low jitter clock generator (Jitter~1ps) to drive the GTP tiles.
➢ To test the links, frame generators are used to organize the data in frames and forward them to the transmitters. The data are looped back to the receivers and both sets of data are forwarded to the corresponding frame checker for validation.
➢The Xilinx ChipScope software is used to monitor and control the design . That tool handles and shows stimulus in the intergraded on chip logic analyzer. The error_count signal validates a good data transition.


The MP7 card

Controls and monitors the virtual IOs | Controls the Trigger properties | The signals are shown


Xilinx ChipScope pro Analyzer tool

The μTCA Crate

Implementation

1.With Synchronous clocks

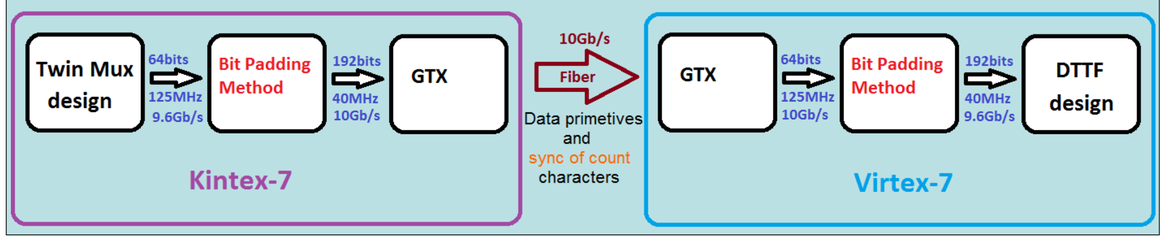
In synchronous operation the transceiver clock has to be a multiple of the DTTF algorithm clock (bx time). The GTH transceivers[4] of some Virtex-7 FPGAs are operational in 9.6Gb/s. In that rate the GTHs serves a 64bit bus at 120MHz and therefore the GTH clock is 3 times the bx time (3X40MHz =120MHz).

2.With Asynchronous clocks

Some Virtex-7 and all the Kintex-7 FPGAs do not support GTH transceivers but they have GTXs instead of them. The GTXs have a forbidden gap in the line rate between 8Gb/s and 9.8Gb/s and therefore the GTX must be asynchronous. The line rate in that case is 10Gb/s and a Bit Padding Method is applied to the GTX bus and modifies the rate according to the bx rate. This costs some additional latency (to be defined). The GTX at 10Gb/s have a 64bit bus at 125MHz and the GTX clock is less than 3 times the bx time (40 MHz).

Bit Padding Method

The logic is based on state machines, counters, multiplexers and some registers. The counters of both the transmitter and receiver must be synchronous and a sync of count character is used.



Summary

A new common activity of the HEPLAB, University of Ioannina and of the Institute of Accelerating Systems and Applications, Athens is presented concerning the new DTTF architecture for the CMS Trigger Upgrade. Legend Xilinx FPGAs with GTPs, are already running at the top line rate (3.2Gb/s each). Soon new hardware capable of 10Gb/s will be used.

Two options are used to design the new transceivers, synchronous and asynchronous. At the asynchronous mode a Bit Padding Method is used.

References

[1] CMS collaboration, The TriDAS Project – The Level-1 Trigger Technical Design Report, CERN-LHCC-2000-38 (2000).
[2] H. Bergauer et al., Drift Tube Muon Trigger Track Finder System (DTTF System), J. Erö (editor), Report submitted to GT/GMT/DTTF Review Committee, Vienna, Austria (2004), http://wwwhephy.oeaw.ac.at/p3w/cms/trigger/Review/Information/DTTF_Description_1.0.pdf.
[3] http://www.xilinx.com/support/documentation/user_guides/ug386.pdf
[4] http://www.xilinx.com/support/documentation/userguides/ug476_7Series_Transceivers.pdf

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