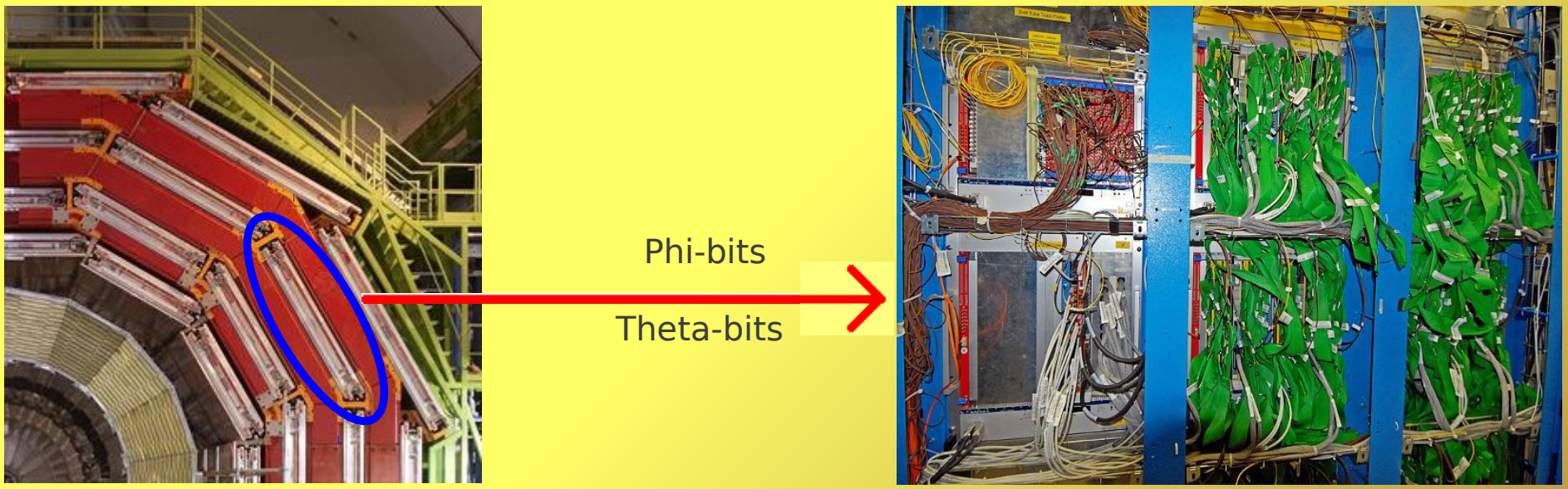
DTTF inputs - Discussion



The **Minicrate - DTTF** trigger chain

THE UNIVERSITY OF IOANNINA

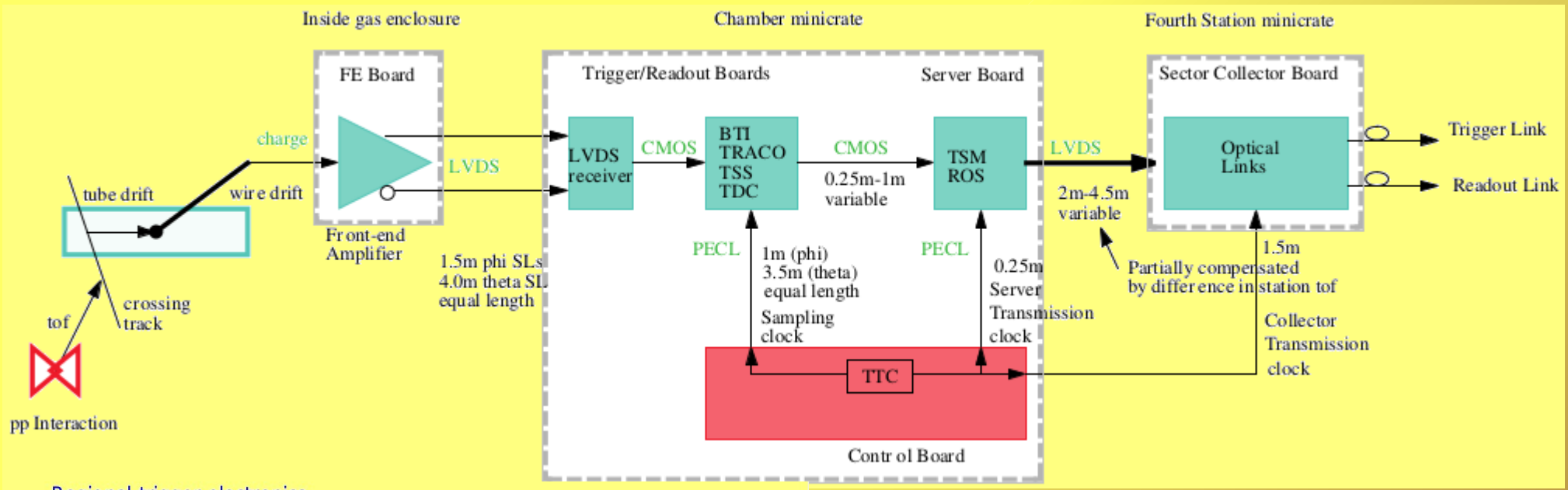
High
Energy
Physics
LABoratory

Nikitas Loukas - Phd Student

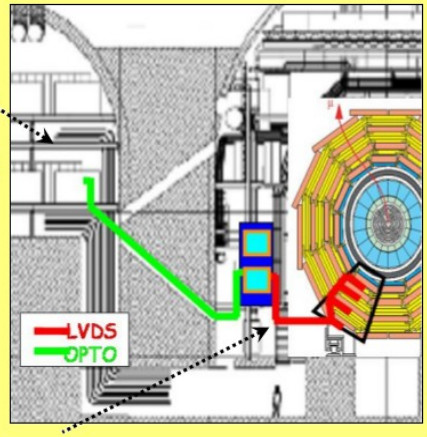
Outline

- General Overview
- MINICRATE
  - Trigger primitives generation
  - Local Trigger Output
- Sector Collector
  - Current architecture
  - New architecture
  - Minicrate – DTTF trigger chain
- The DTTF Baseline
- Drift Tube Track Finder inputs

General Overview



Regional trigger electronics
(underground counting room)



SC Output links :
6 optical @ 1.6 Gbit/s per link
1 GOL chip per link

SC Input links :
Cat-5 FTP cables
(480 Mb/s LVDS) :
2 copper cables/chamber
4 twisted pairs/cable

Located on detector towers,
60 SC boards (1/DT 30° sector),
2 VME 9U crates / wheel

- Signal generation - DT cells
- Track identification and signal digitization
- Local trigger processing
- Data multiplexing and transmitting
- Sector Collector Outputs – DTTF Inputs

Trigger primitives generation

DT Local Trigger

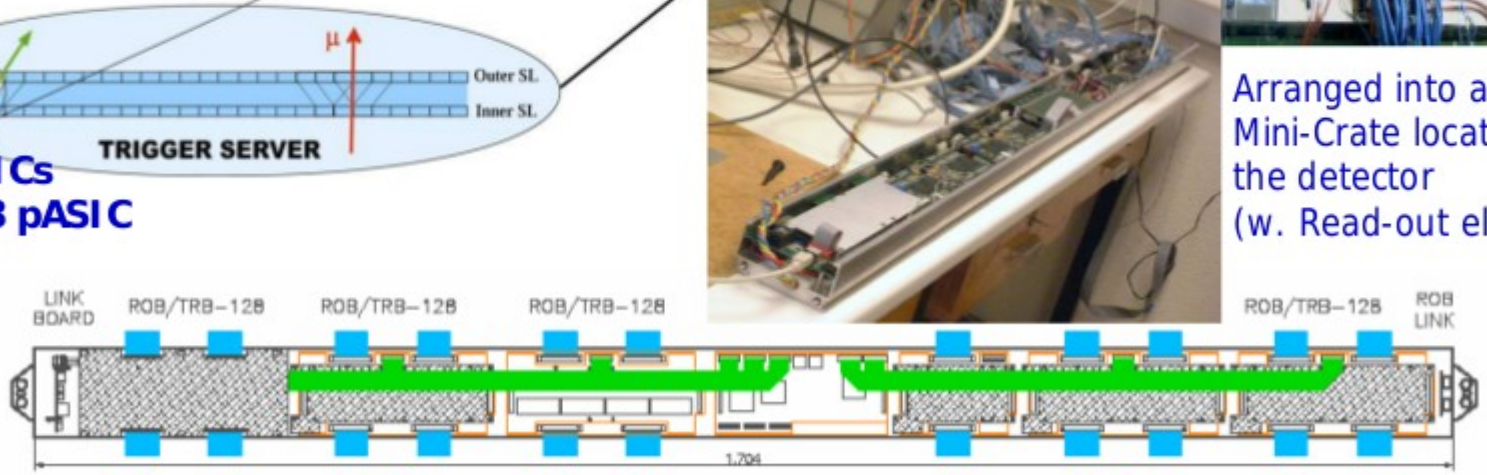
~40000 ASICs

~4400 ASICs

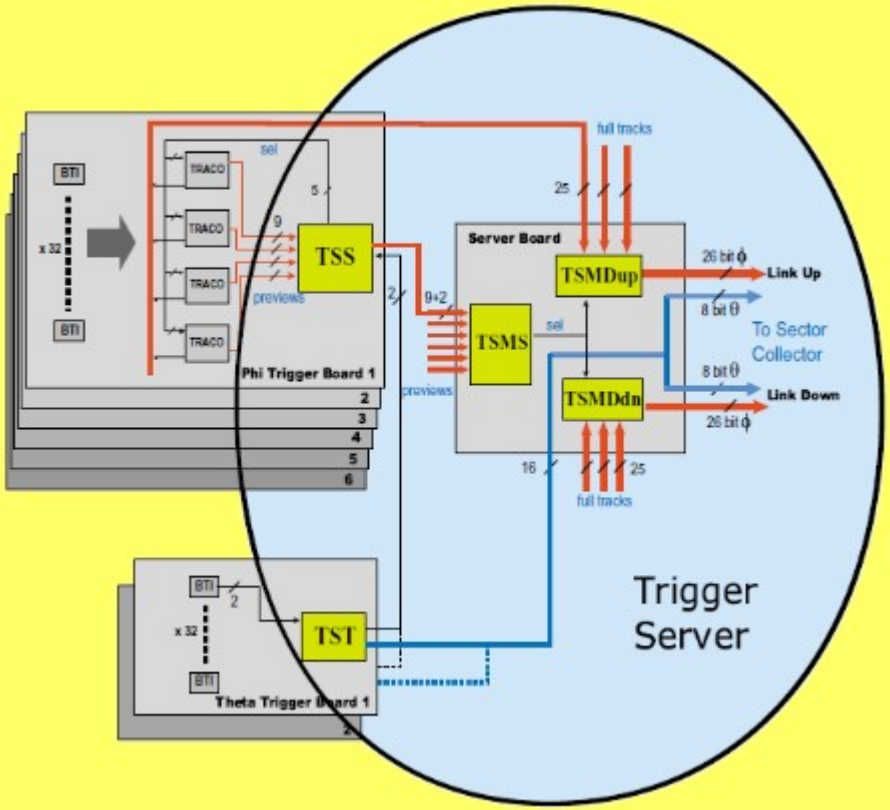
1200 ASICs + 250 x3 pASIC

- **Synchronous pipelined system** (40 MHz)
- Processing stages organized in a logical tree structure

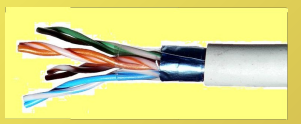
Arranged into a Mini-Crate located on the detector (w. Read-out elctr.)



Local Trigger Output
(MINICRATE)



Data	Width (bits)	Type & comments
ϕ_r up track	12	signed, 1-compl.
ϕ_b up track	10	signed, 1-compl.
Quality up track	3	see table 3.4
$1^{st}/2^{nd}$ up track	1	
ϕ_r down track	12	signed, 1-compl.
ϕ_b down track	10	signed, 1-compl.
Quality down track	3	see table 3.4
$1^{st}/2^{nd}$ down track	1	
θ triggers	8	
θ quality	8	H/L for each trigger bit
Bunch Crossing 0	3	From up, down and θ
Bunch Crossing count	2	2 LSbits of the bunch counter
Parity ϕ data	2	Up and down
CCB info	4	Minicrate Control Board status
Trigger output	1	Chamber autotrigger

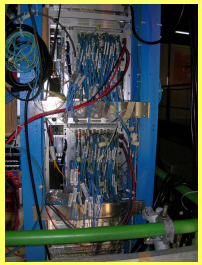
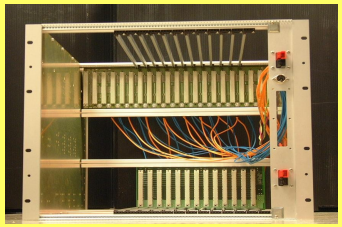
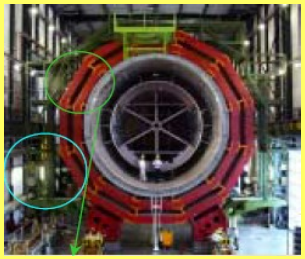
2 X 

8 LVDS links
80 bit/BX
per chamber

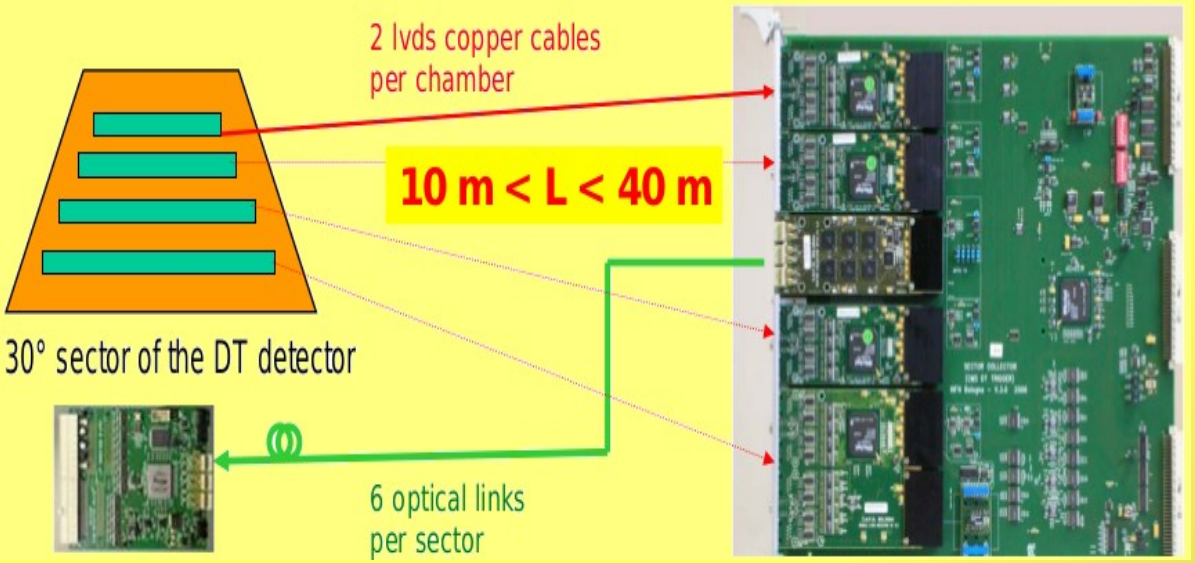
320 bit/BX
12.8 Gb/s per sector (4 ch.)

FTP Cables	LVDS links	data	Trigger data	Chambers (MINICRATE)	Sectors	Data rate	Trigger data rate
-	1@480Mbps	12 bits	10 bits	-	-	0.48 Gbps	0.4 Gbps
1	4@480Mbps	48 bits	40 bits	-	-	1.92 Gbps	1.6 Gbps
2	8@480Mbps	96 bits	80 bits	1	-	3.84 Gbps	3.2 Gbps
4	16@480Mbps	192 bits	160 bits	2	-	7.68 Gbps	6.4 Gbps
8	32@480Mbps	384 bits	320 bits	4	1	15.36 Gbps	12.8 Gbps
16	64@480Mbps	768 bits	640 bits	8	2	30.72 Gbps	25.6 Gbps
480	1920@480Mbps	23040 bits	19200 bits	240 full barrel	2 X 30 = 60	921.60 Gbps	768.0 Gbps

Twin Mux "SC"

Sector Collector
Current architecture



- 10 VME crates at the balcony
  - 60 Trigger Sector Collector (TSC)
- LVDS-RX mezzanine card
  - 2CablesX4LVDSat480Mbps=3.84Gbps
  - TSC input = 4X(2X4at480Mbps)=**15.36Gbps**
- OPTO-TX mezzanine card
  - 6at1.6Gbps(32b/40b_encoding)=**7.68Gbps**
- **Hence, 320bits/BX output for 160bits/BX output???**

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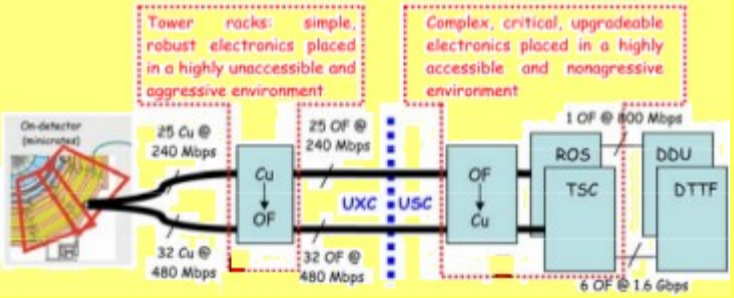
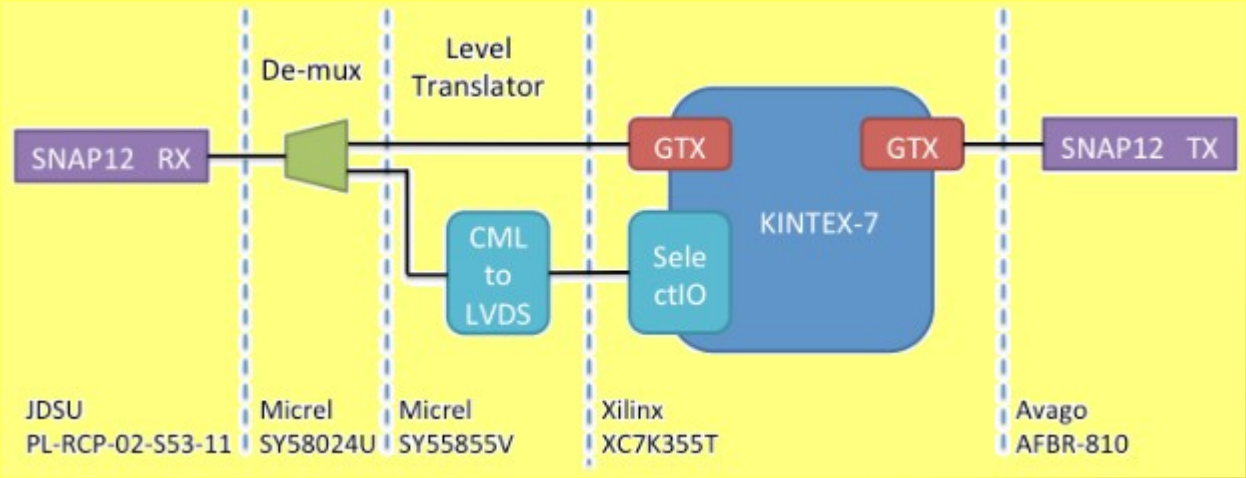
480	1920@480Mbps	23040 bits	19200 bits	240 full barrel	5 X 12 = 60	921.60 Gbps	768.0 Gbps

Sector Collector
New architecture (Twin Mux)





- 3 uTCA crates, 10 uTCA cards each (3 X 10=30)
- SNAP12-RX Input (2 Sectors input data per card) — 640 bits
  - One chamber: 2X4at480Mbps = 3.84Gbps, so
  - Two Sectors : 8(2X4at480Mbps) = **30.72Gbps ???**
    or : 0.8X(12at1.6Gbps) = **15.36Gbps ???**
- SNAP12-TX Output (3 copies of the 2 Sectors) — 320 bits
  - Output per Chamber
    - 34 bit/BX to PHTF and 19 bit/BX to ETTF
  - Output per Sector (4 Chambers)
    - 136 bit/BX to PHTF and 76 bit/BX to ETTF
    - 5.44Gbps PHTF + 3.04Gbps ETTF = 8.48Gbps
    - Full throughput Required 12.8Gbps → **15.36Gbps**

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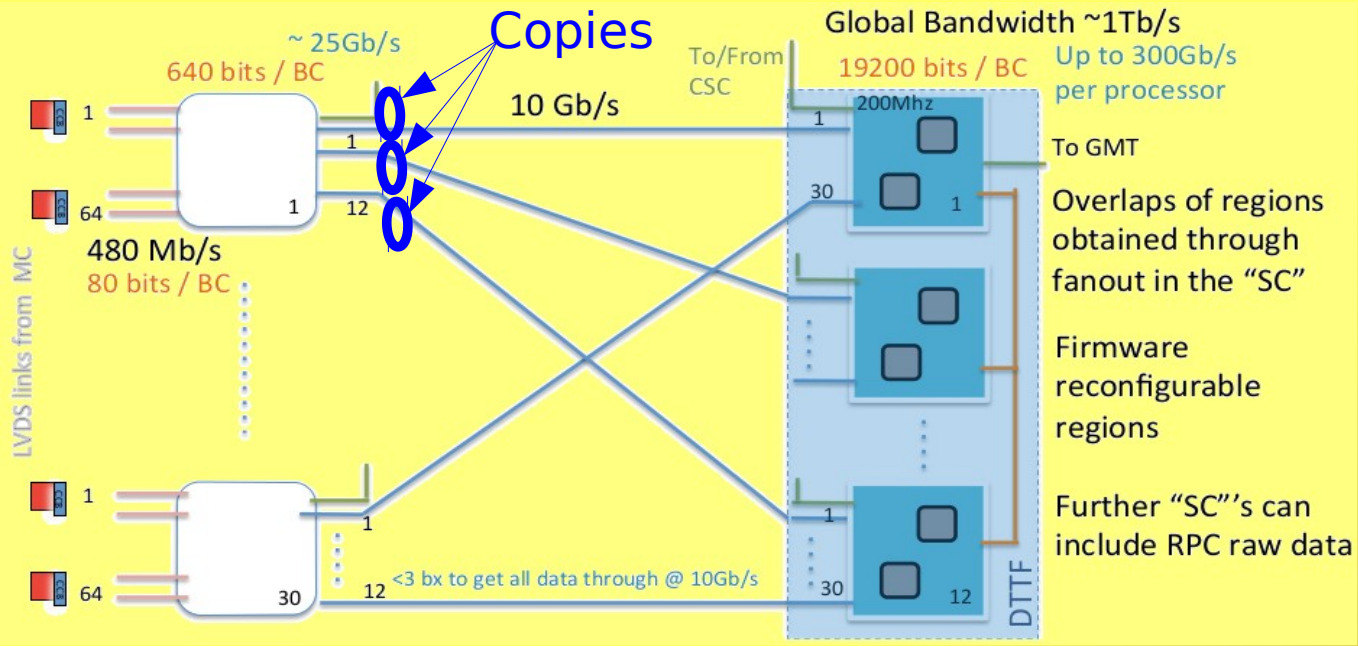
Twin Mux "SC"

Minicrate → DTTF trigger chain



- 240 Chambers
- 30 Twin Mux SCs
  - 640bits X 30SC = 19200bits
- 12 DTTF processors
- **Kindex 7 GTX 9.6 Gbps ???**
  - Twin Mux SC output
    - 12 links at 9.6Gbps (3 Copies of 2 Sectors)
    - **4at9.6Gbps** →640bits concerning 2 Sectors
    - **8at9.6Gbps** →2X640bits copies for neighbors
  - DTTF cards input
    - 192bits X 30links = 5760bits
    - 30at9.6Gbps=**288Gbps** → 230.4Gbps
    - 230.4Gbps / 40MHz=**5760bits**
- 12crates X 230.4Gbps = 2764.8Gbps
- 2764.8Gbps / 3Copies = **921.6Gbps**

Kintex-7 (Speed Grade -2) 0.5 - 8 Gbps and 9.8 - 10.3125Gbps

FTP Cables	LVDS links	data	Trigger data	Chambers (MINICRATE)	Sectors	Data rate	Trigger data rate
-	1@480Mbps	12 bits	10 bits	-	-	0.48 Gbps	0.4 Gbps
1	4@480Mbps	48 bits	40 bits	-	-	1.92 Gbps	1.6 Gbps
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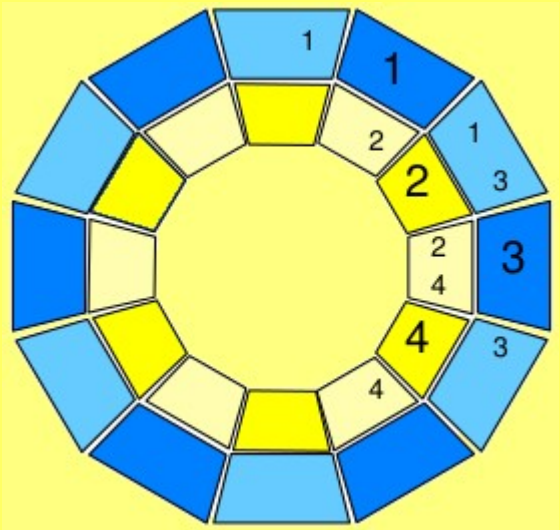
Twin Mux "SC"

DTTF Baseline



- Each processor is mapped to one full wedge plus its two neighbor wedges
- 9.6Gbps, 192bit/BX (2links forwards 1sector's data)
  - INPUTS
    - 24 links own Sector
    - 12 links neighbor Sector
    - 4 links CSC
  - OUTPUTS
    - 4 links CSC
    - 3.5 links Trigger out
    - 0.14 links DAQ out
- 30 input links divided by 2 links means 15 Sectors
- But 15 Sectors are excactlly 3 Wedges
- So, the 30@9.6Gbps links are the full barrel input needed.

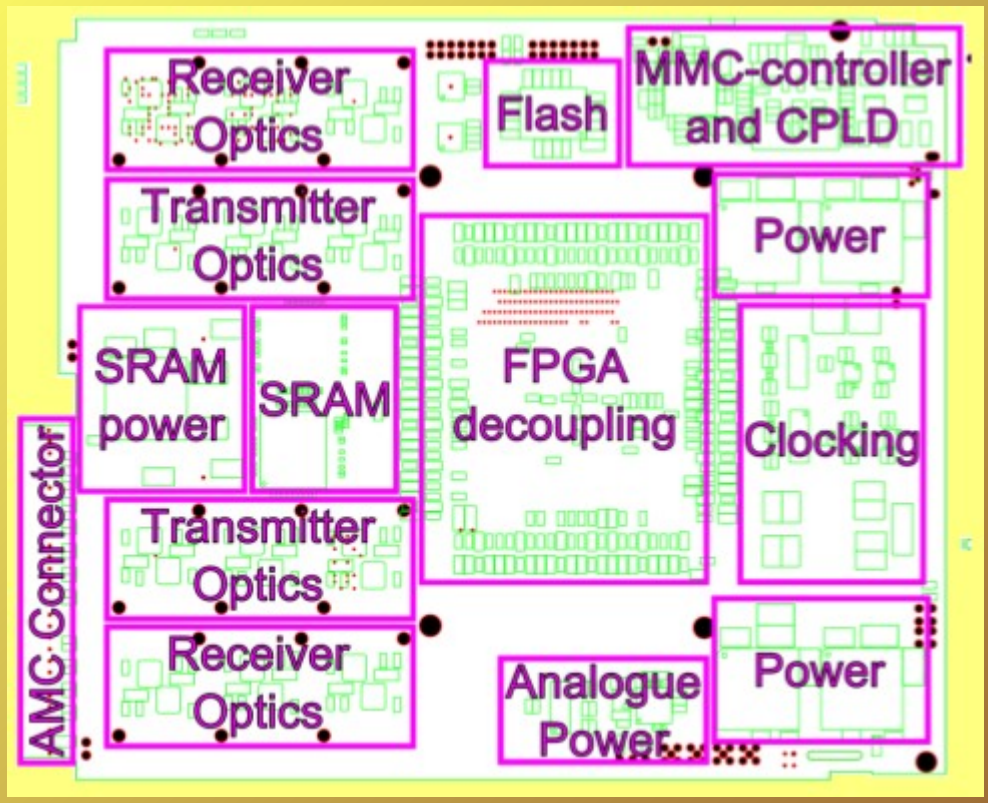
Two Full Wedges	PHTFs	ETTFs				HiSpeed			NBspeed			Tr. speed			DAQ speed			Total GTX	
all Chamber data	12.0	2.4				9'600			9'600			3'200			3'200			HiS fanout input	
with 9.6Gbps links				Input			CSC		Neighbor										
	LE	Memory	Regs			HiSpeed	IN	OUT	IN			Trigger out			DAQ out			BP	Front
		kbit		bit/BX	Mbit/s	links	links	links	bit/BX	Mbit/s	links	bit/BX	Mbit/s	links	bit/L1A	Mbit/s	links		
	521'880	12'322	270'180	3'840	153'600	20	4	4	3'840	153'600	20	224	8'960	3.5	3'571	357	0.14	5	44

Four Half Wedges	PHTFs	ETTFs				HiSpeed			NBspeed			Tr. speed			DAQ speed			Total GTX	
all Chamber data	12.0	2.4				9'600			9'600			3'200			3'200			HiS fanout input	
with 9.6Gbps links				Input			CSC		Neighbor										
	LE	Memory	Regs			HiSpeed	IN	OUT	IN			Trigger out			DAQ out			BP	Front
		kbit		bit/BX	Mbit/s	links	links	links	bit/BX	Mbit/s	links	bit/BX	Mbit/s	links	bit/L1A	Mbit/s	links		
	521'880	12'322	270'180	4'608	184'320	24	4	4	2'304	92'160	12	224	8'960	3.5	3'571	357	0.14	5	40

Drift Tube Track Finder inputs Conclusions

- There are will be 3 uTCA Crates with 4 DTTF cards on it
- The 12 DTTF card will receive distributed data from SCs
- The SCs will make copies of them for the neighbors
- All the links will run at 9,6Gbps. That means 192bit/BX
- Two links will route data concerning one Sector (384b/BX)
- Each SC will serve two Sectors
- SC will transmits 12 links via Kintex-7 GTXs
- The DTTF will be host in Virtex-7 FPGAs in MP7 cards and the DTTF upgrade team is going how.

The MP7



Additional Slide (How to compute data rates and data widths)

- Data Rate for one link
  - Cable : $Bandwidth = N_{bits} \times \tau_{transmission}$
  - Optical : $Bandwidth = N_{bits} \times \varepsilon_{encoding} \times \tau_{transmission}$
    - $\varepsilon_{encoding} \rightarrow$ 8b/10b encoding
- Data Width $N_{bits} = N_{links} \times W_{link} \times R \times \varepsilon_{encoding} \times \tau_{transmission}$
  - N_{bits} : Number of bits
  - N_{links} : Number of input links
  - W_{link} : Number of channels per link (usually 1)
  - R : Line – speed of the links
  - $\varepsilon_{encoding}$: Efficiency of the encoding scheme (usually 0.8)
  - $\tau_{transmission}$: Transmission period (BX time, 25ns)